

# Semiconductor IP

## 14-bit ADC/VGA, 40 MSPS, TSMC 180 nm IP Core

Industry-Standard, High-Performance,  
Silicon-Proven ADC Technology

- 14 bits of resolution
- 40 MSPS sampling rate
- TSMC 180 nm Mixed Mode process
- 3.3 V analog supply voltage
- 3.3 V digital I/O supply voltage
- Differential input
- Pipeline architecture
- 4-bit variable gain
- Includes complimentary license of patented **PKChek** die level process monitor yield improvement solution

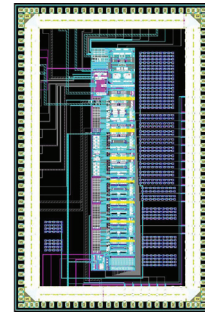


Figure 1: GDSII image of a single-channel ADC

### General Description

Ridgetop's silicon proven ADC is optimized for high performance imaging applications and other high data rate, high SNR applications. This ADC is designed for the TSMC 180 nm Mixed Mode process using MIM capacitors. The ADC is fully differential variable gain input, and has pipeline architecture with 1.5 bits-per-stage resolution, with digital error correction. Each stage makes two conversions per clock cycle resulting in a 2-bit output. The architecture allows individual ADC stages to be scaled and optimized for both noise and power. Figure 1 shows GDSII layout, Figure 2 illustrates the ADC pipeline architecture, and Table 1 outlines the ADC specifications.

### Applications

- Medical imaging
- Digital radio
- Detectors
- Instrumentation

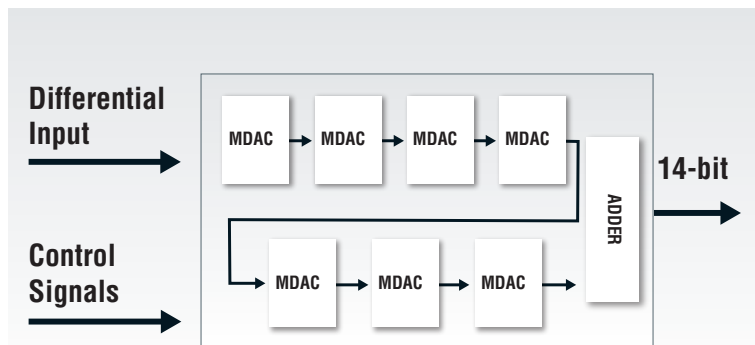


Figure 2: ADC pipeline design - seven MDAC stages, 1.5 bits per stage

**Table 1: Summary of ADC Core Specifications**

PARAMETER	SPECIFICATION	NOTES
Accuracy	14-bit resolution (12.5-bit accuracy)	
Sampling rate	40 megasamples per second (MSPS)	
Digital output data format	14-bit parallel @ Fs (single-ended)	
Analog supply voltage	3.0 V (min), 3.3 V (typ), 3.6 V (max)	
Digital supply voltage	3.0 V (min), 3.3 V (typ), 3.6 V (max)	
Analog input voltage	2 V peak-to-peak (differential)	
Input capacitance	3 pF	
Input reference voltage	1.22 V (typ)	
Power consumption	~53 mW	1
Temperature range	-40 to +85 °C	2
Latency	9 clock cycles	3
Differential non-linearity (DNL)	1-2 LSB	
Integral non-linearity (INL)	1-2 LSB	
Area per channel (excluding V ref block and pads)	1.7 mm <sup>2</sup>	1
Process	TSMC 180 nm (CM018)	

**NOTES**

1	Includes VGA
2	Temperature may cause roll-off in specifications
3	Customer will supply clock signal to ADC IP Block
4	Includes complimentary license for <a href="#">PDKChk</a>

**Need modified or custom design? Contact Ridgetop at 520-742-3300 to discuss your ideal solution!**

Copyright © 2009 Ridgetop Group Inc. All rights reserved. Other products mentioned may be trademarks or registered trademarks of their respective holders. The information contained herein is subject to change without notice.

**Corporate Headquarters**

6595 North Oracle Road  
Tucson, Arizona 85701 USA  
OFFICE +1 520 742 3300  
FAX +1 520 742 1111

**Worldwide Locations**

Support and sales locations for Ridgetop Group Inc. exist in Germany, Belgium, Japan, China, Canada, and the United States.  
For office locations and contact information, please call the corporate headquarters or visit us on the web: [www.ridgetopgroup.com](http://www.ridgetopgroup.com).