

Application Note | AN105

Flip-Chip Interconnection Integrity Testing Solutions

Introduction

This application note describes interconnection reliability problems, provides the flip-chip solution overview, and includes test application considerations. Flip-chip refers to a packaging technique for interconnecting semiconductor devices, such as IC chips and microelectromechanical systems (MEMS), wherein the active (top) area of the chip faces downward and any part of its surface area can be used for interconnection. Flip-chips enable a larger number of interconnects in shorter distances than conventional wire-bond chips.

Statement of Problem

Interconnect reliability problems are commonly experienced when using large ball grid array (BGA) packages with embedded flip-chip devices. The reliability issues are primarily related to the on-chip interconnect in the following ways:

- stacked vias used in flip-chip-to-substrate interconnect (solder bumps)
- packaging/package assembly process
- package-to-board interconnect (to a lesser extent)

This application note explains the reliability aspects (involving cracking and delamination) of the different parameters involved in the interconnect chain; i.e., on-chip interconnects – chip-to-substrate interconnect (bumps), and substrate-to-board interconnect (balls).

Two solutions can be provided using IP, expertise, and instrumentation available from Ridgetop Group and Ridgetop Europe (Q-Star Test). The solutions are Ridgetop's SJ BIST™ interconnect reliability monitor and Q-Star's PG-Mon interconnect reliability monitor. These solutions, detailed in the sections that follow, can be used to gather reliability information on the different aspects of the interconnect path.

Solution Overview

Both the SJ BIST and PG-Mon reliability observation monitors are based on the observation that reliability-related issues affect the resistance of the interconnect path being observed. They are inserted at critical reliability points of the system. A combination of SJ BIST with PG-Mon further provides a powerful reliability observation and measurement tool, as PG-Mon can also be linked with the dedicated I/O required by SJ BIST. Both solutions need to be mapped to the target application technology.

Both SJ BIST and PG-Mon are useful for gathering information on the reliability aspects of the interconnect chain as a whole (die-to-board interconnect involving on-chip interconnects; chip-to-substrate interconnect, i.e., bumps; and substrate-to-board interconnect, i.e., balls) as well as for gathering reliability information on sub-aspects of the die-to-board interconnect chain, such as the on-chip interconnect section and the chip-to-substrate interconnects involving the bumps. The ultimate effectiveness of this solution is a function of how the reliability monitors are linked with the interconnect paths to be observed.

SJ BIST

SJ BIST is a small digital IP core that was originally developed to investigate and monitor solder joint reliability on ball grid array (BGA) packages, but it is equally well-suited to investigate and evaluate different aspects of interconnect reliability. SJ BIST makes its interconnect reliability observation by monitoring the amount of charge transferred over a given amount of time between its two observation terminals.

It does this by writing out a sequence of 1's and 0's out of one of its observation terminals and verifying the arrival of the correct sequence at the other observation terminal, and vice versa. (Data is sent back and forth between the two terminals.) A small capacitor connected to the interconnect being observed defines the detection threshold as a function of the data transfer frequency being used. If the reliability of the observed interconnection is affected, causing either increased interconnect resistance or intermittent contact behavior, then this affects the charge transfers between the SJ BIST observation terminals, leading to a failure of the executed test.

Figure 1 illustrates the basic SJ BIST operating principle, showing an FPGA solder ball observation as an example. Figure 2 shows the impact of a fault causing the resistance of the observed interconnect path to increase to 300 ohms. As can be observed, the 300-ohm fault causes a degradation of the charge transfer, resulting in a transmitted 1 not being recognized as a 1 at the observation terminal.

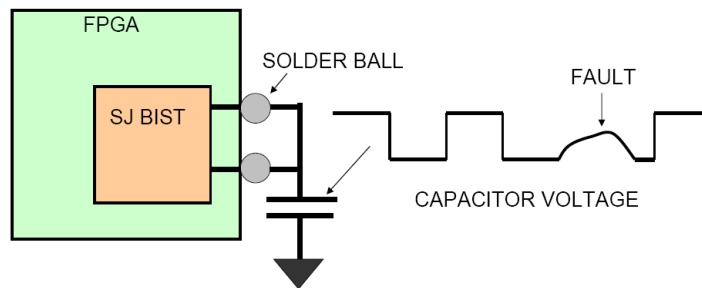


Figure 1: SJ BIST operation principle

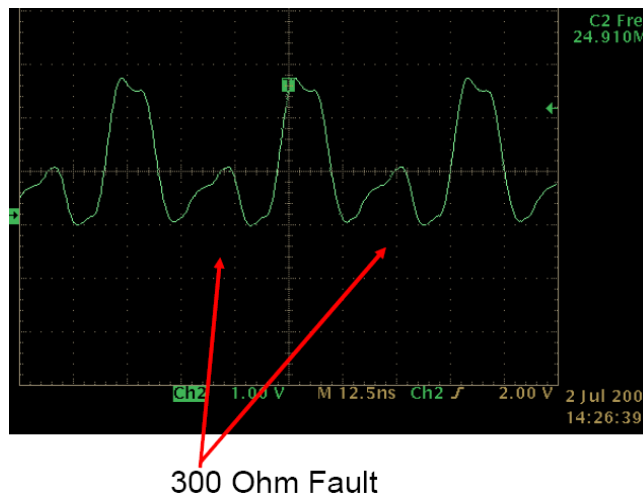


Figure 2: SJ BIST charge transfer affected by a fault causing a 300-ohm interconnect resistance increase

SJ BIST runs stand-alone and can be used to observe the reliability of the interconnect path between its two observation terminals throughout the lifetime of the product in which it is embedded either in a sampled way (at dedicated timing points under control of the user) or continuously (free running mode). SJ BIST can provide diagnostics related to intermittent fault occurrences as well as pass/fail information.

For its operation, SJ BIST requires a dedicated interconnect observation path (connecting its two observation terminals) that may involve dedicated I/O. If on-chip interconnect observation is targeted, then no dedicated I/O is needed. SJ BIST can be used during qualification and also during lifetime observations. The operation of SJ BIST is based on monitoring charge transfers. The rate at which a certain amount of charge can be transferred from one point to another is a measure of the reliability of the interconnection. Different instantiations of SJ BIST allow reliability investigation of different types of interconnect paths: on-chip interconnects (from one interconnect layer to another addressing contact, metal, and (stacked) via reliability), chip-to-substrate reliability (involving on-chip interconnect and chip-to-substrate bump reliability), and chip-to-board interconnect reliability (involving on-chip interconnects, bumps, substrate and balls), as illustrated in Figure 3.

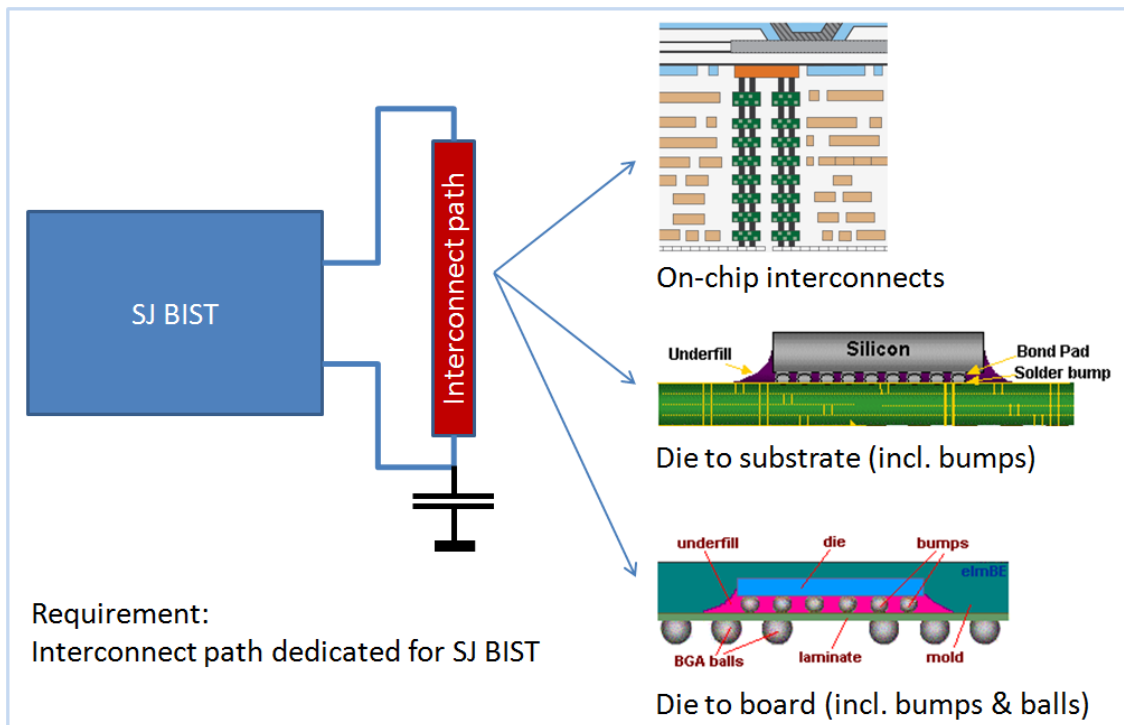


Figure 3: SJ BIST application concept

PG-Mon

PG-Mon is a small analog core consisting of an observation circuit and a small switch serving as current source or sink, to enable the interconnect reliability observation. The PG-Mon core is robust and process parameter variation-independent by design. PG-Mon was originally developed to investigate reliability of individual branches (that are typically hooked up in parallel) making up the power and ground connections of an integrated circuit, but it is equally well-suited to investigate and evaluate general interconnect reliability.

PG-Mon is nonintrusive to the function of the circuit and is designed to coexist with a functional on-chip interconnect and/or I/O path, and hence does not require dedicated interconnects or dedicated I/O for its reliability observation. The PG-Mon base principle is illustrated in Figure 4. Figure 5 shows an example PG-Mon implementation. The PG-Mon observation core taps onto the

interconnect being observed, and uses the intrinsic resistance of the interconnect between its two observation points, as sense resistance. PG-Mon is designed to work with a very low-sense resistance, requiring no special sense resistor insertion but exploiting the sheet resistance of the interconnect material being used between its two observation points.

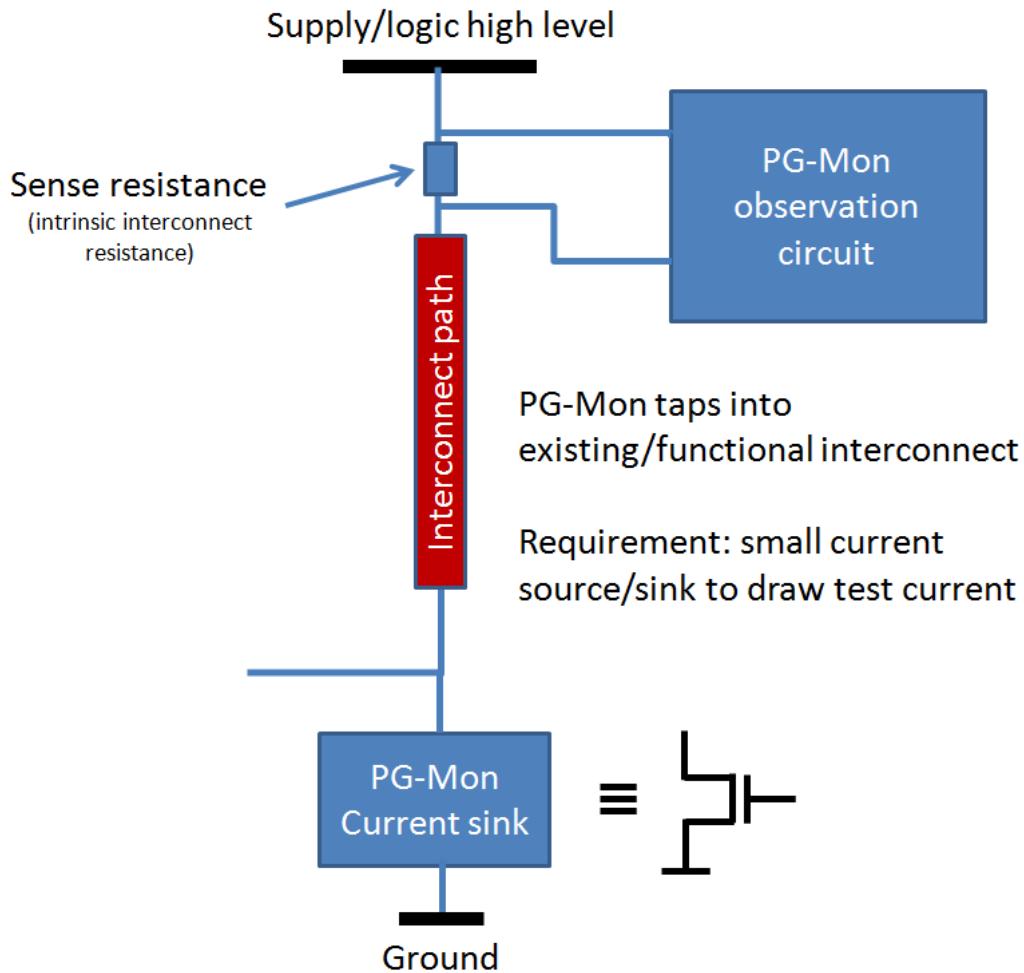


Figure 4: PG-Mon basic application

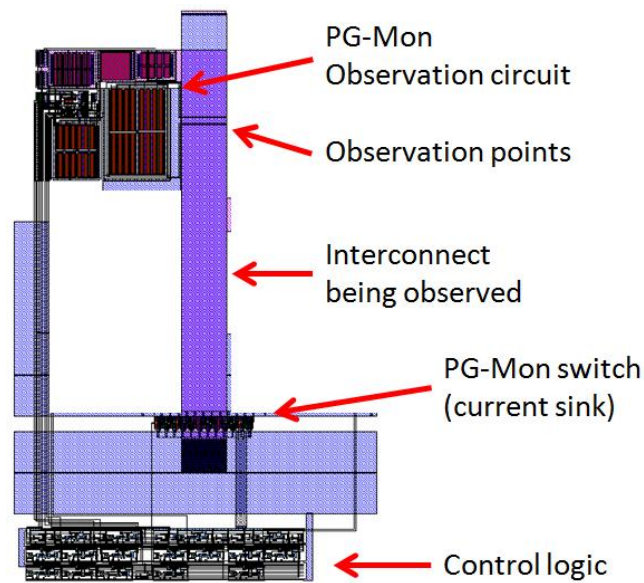


Figure 5: Example PG-Mon implementation

The operation of PG-Mon is based on a differential current measurement, making use of a controlled current source or current sink depending on the interconnect path being observed. The controlled current source or sink is actually a small transistor switch. The switch in combination with the PG-Mon observation circuitry makes up the PG-Mon reliability monitor. A PG-Mon-based interconnect reliability observation involves two measurements: At first a measurement is done with the controlled current source/sink not active (open switch), serving as a reference measurement. Secondly a measurement is done with the controlled current source/sink active (closed switch). The difference between the two readings yields the PG-Mon pass/fail decision.

The resistance of the interconnect path determines the actual current flowing when the switch is closed, hence an increase in resistance over time of the interconnect being monitored will lead to a transition from a pass result (observation at time₁) to a fail result (observation at time₂), monitoring the interconnect reliability over time.

A requirement for PG-Mon is that the interconnect under investigation can be made subject to a current flow. As such, when no measurement observation is performed, PG-Mon can coexist with the (functional) interconnect path to be monitored without affecting the functional operation of the circuit. PG-Mon requires a test mode operation of the circuit to enable its measurement, yielding a "sampled" observation mode, i.e., the circuit is put in test mode from time to time to support the reliability tests. Reliability tests are, for example, run as part of the circuit power-on procedure.

An alternative configuration is to attach PG-Mon to a dedicated (nonfunctional) interconnect path to be observed. In such a case the PG-Mon reliability observation can run concurrently with the normal circuit operation and a continuous interconnect reliability observation can be made.

PG-Mon can be used not only to qualify/verify the reliability of a single interconnect path, but also to validate the reliability of a set of parallel interconnects. This enables identification of which of the interconnects making up the parallel path are in good shape and which ones are faulty. In such case, a PG-Mon observation circuit is to be attached to each branch making up the parallel interconnect.

Similar to SJ BIST, different instantiations of PG-Mon allow reliability investigation of different types of interconnect paths: on-chip interconnects (from one interconnect layer to another addressing contact, metal and (stacked) via reliability), chip-to-substrate reliability (involving on-chip interconnect and chip-to-substrate bump reliability), and chip-to-board interconnect reliability (involving on-chip interconnects, bumps, substrate and balls), as illustrated in Figure 6.

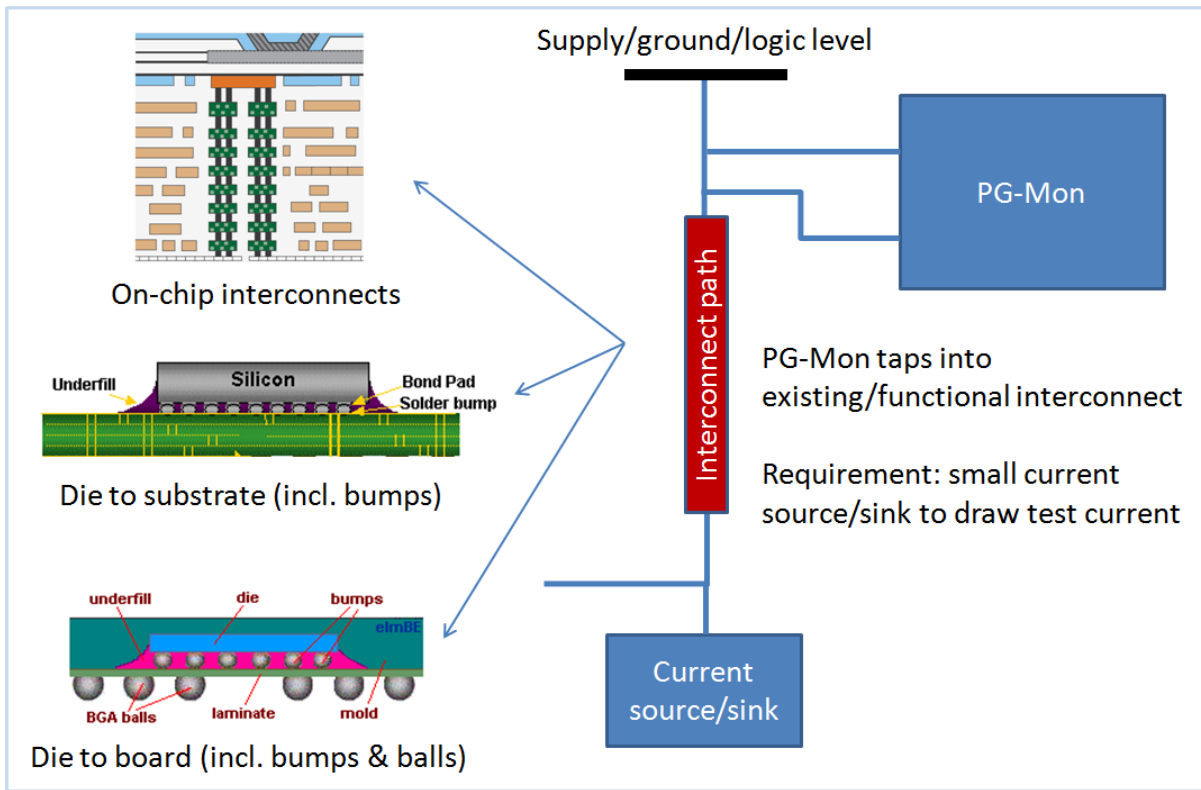


Figure 6: PG-Mon application concept

PG-Mon and SJ BIST can be further combined into a more advanced interconnect reliability monitor, as illustrated in Figure 7.

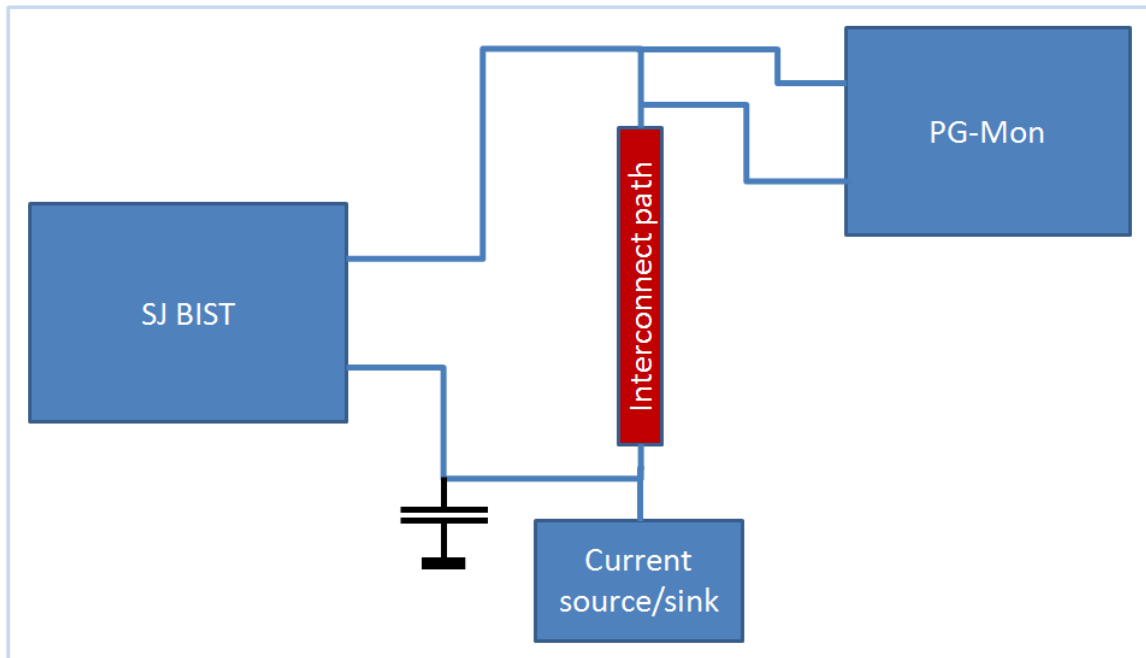


Figure 7: Combined SJ BIST/PG-Mon application concept

Table 1 details the differences between the features of SJ BIST and PG-Mon.

Table 1: SJ BIST and PG-Mon Features

FEATURE	SJ BIST	PG-Mon
Core type	Digital	Analog
Observation	Charge-based	Current-based
Coexistence with functional interconnects	No – requires dedicated interconnects	Yes – can coexist with functional interconnects
Operation mode	Sampled or Continuously	Sampled – if linked with a functional interconnect, requires a test mode operation for making its observation Sampled or Continuously – if linked with a dedicated interconnect.
Operation concurrency	Yes – can operate concurrent with other circuit functions	No – if linked with a functional interconnect, requires a test mode operation for making its observation Yes – if linked with a dedicated interconnect
Sensitivity (change in resistance)	100 to 500 ohms – a better sensitivity can possibly be achieved by an appropriate selection of operating frequency and loading capacitance.	1 to 5 ohms
Detection of intermittences	Yes	Possibly – if they occur during the measurement phase
Technology adaptation	Simple (digital design)	More complex (analog design)
Output	Diagnostic information Pass/fail flag	Pass/fail flag

Application Considerations

Both SJ BIST and PG-Mon allow reliability investigation of different types of interconnect paths: on-chip interconnects (from one interconnect layer to another addressing contact, metal and (stacked) via reliability), chip to substrate reliability (involving on-chip interconnect and chip-to-substrate bump reliability) and chip-to-board interconnect reliability (involving on-chip interconnects, bumps, substrate and balls), as illustrated in the figures that follow Figure 8 through Figure 13.

Combining their functionality yields a very powerful reliability monitor.

Note: The SJ BIST logic core/PG-Mon core arrow in Figure 8 through Figure 13 is pointing to the active area of the silicon, indicating that SJ BIST and/or PG-Mon core are part of the chip and embedded in the silicon.

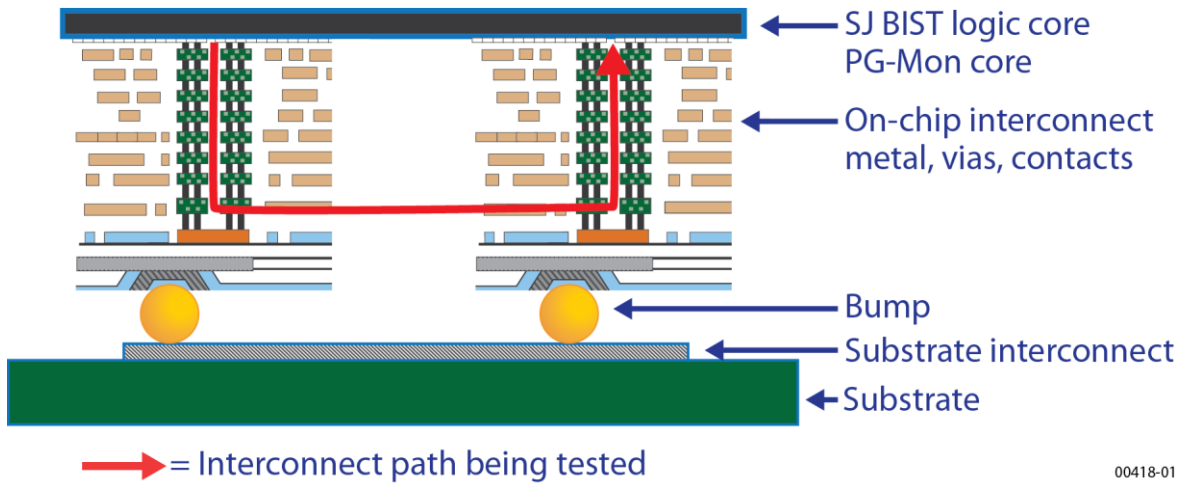


Figure 8: On-chip reliability interconnect verification

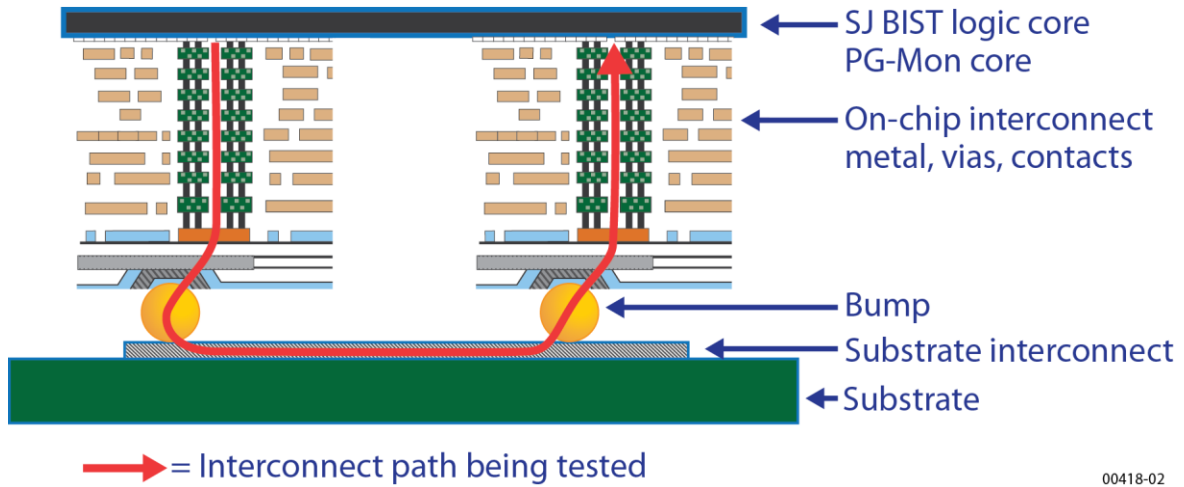


Figure 9: Die-to-substrate interconnect reliability verification

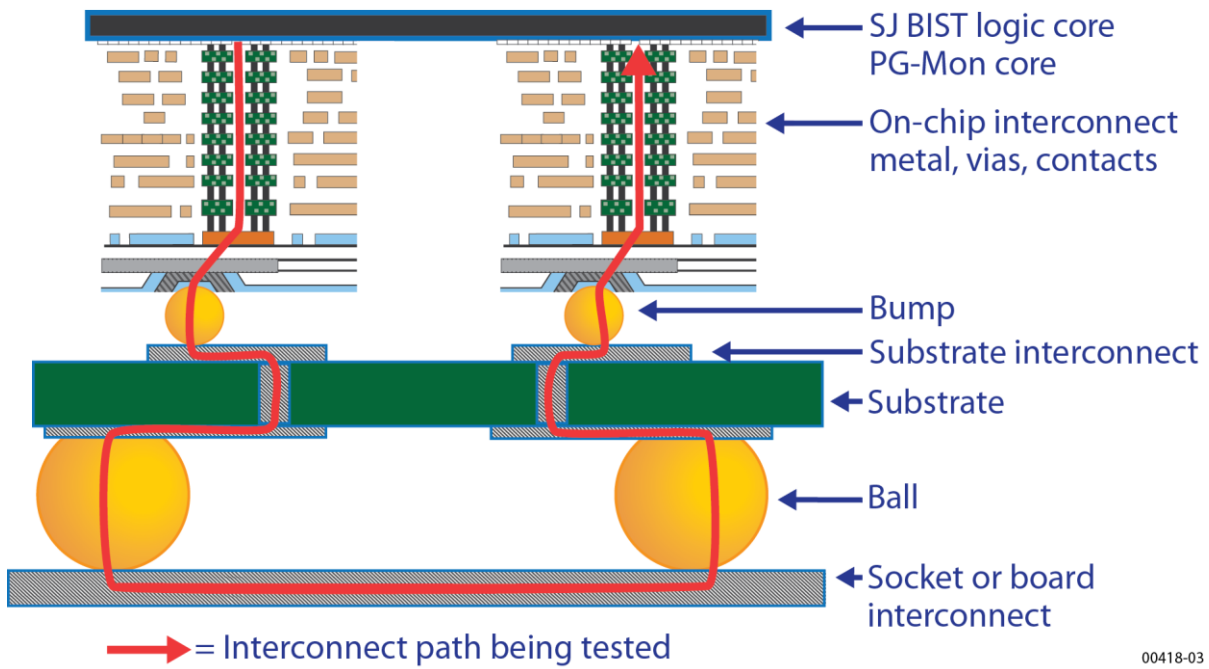


Figure 10: Die-to-board reliability verification

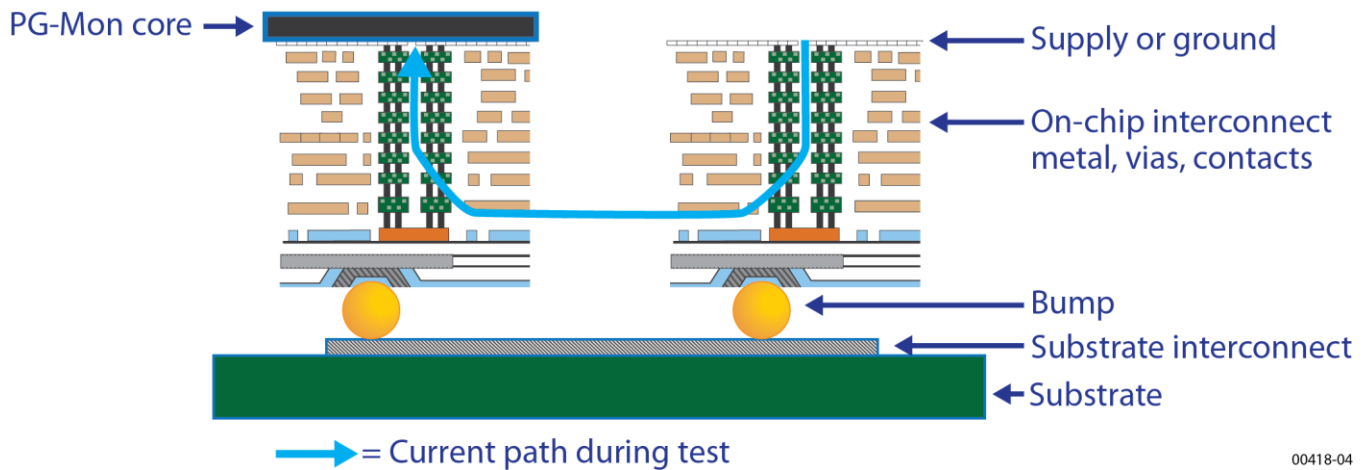
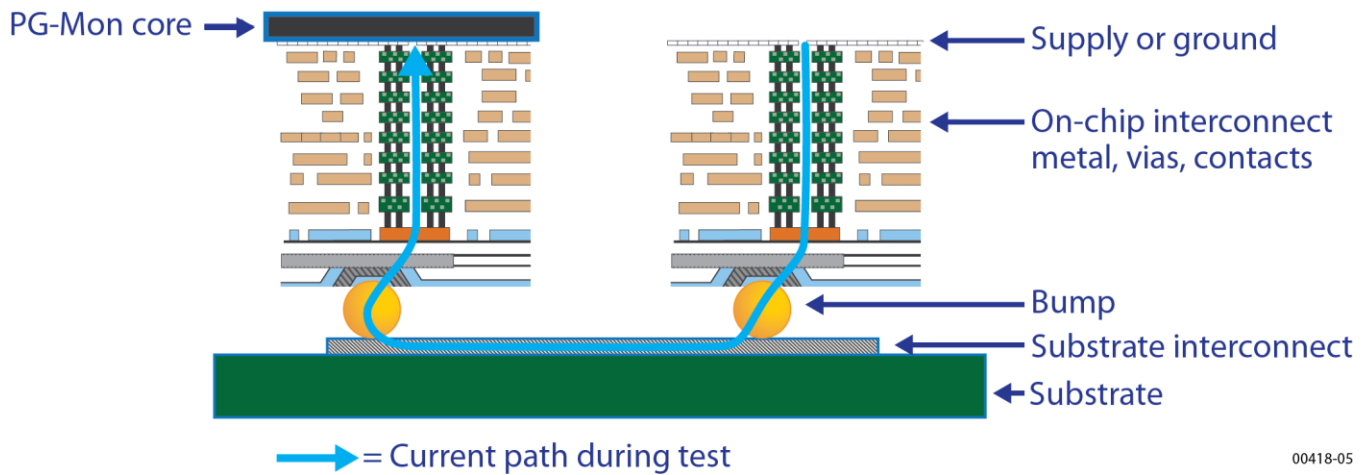
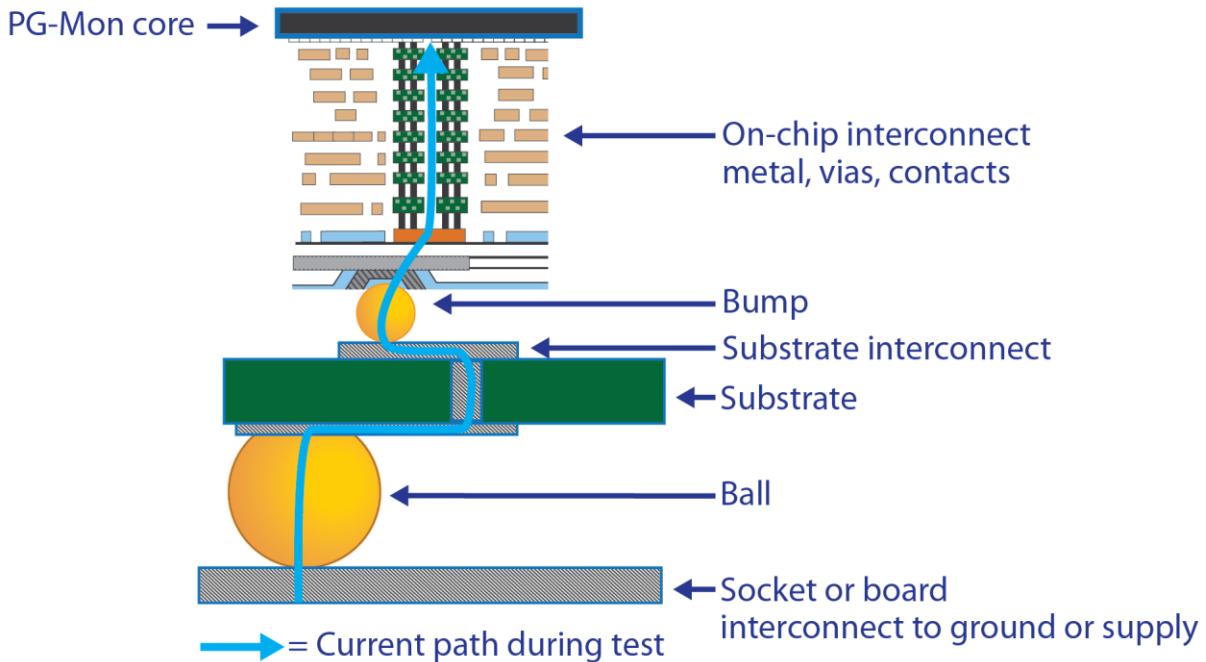


Figure 11: PG-Mon on-die interconnect reliability verification



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Figure 12: PG-Mon die-to-substrate interconnect reliability verification



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Figure 13: PG-Mon die-to-board interconnect reliability verification

To operate and control the SJ BIST circuit, a minimal set of control signals is needed. If SJ BIST is used in continuous observation mode, then only a clock signal and a pass/fail output are required. If SJ BIST is used in a sampled diagnostic operating mode, then a measurement-enable and an output shift control signal are needed as well.

PG-Mon requires a measurement control signal and a pass/fail output.

With a small amount of additional logic, both circuits can easily be linked to and controlled by an already present JTAG port, requiring no additional circuit I/O.

Making use of a switch matrix between the reliability observation monitor (SJ BIST or PG-Mon) and related switch control logic allows reliability observations of different interconnect paths using only one reliability monitor core, avoiding the need for different monitor instantiations to observe different interconnect paths. For example, a switch matrix could control a simultaneous implementation of the paths described in Figure 11, Figure 12, and Figure 13. Each path could be observed at separate times and then reported on individually.

Conclusion

Solutions for ongoing monitoring of interconnection reliability in advanced flip-chip package types have been presented. SJ BIST is useful as a digital implementation, and PG-Mon provides a precision analog approach. The products can be used separately, or together to provide a comprehensive testing solution. Contact Ridgetop Group for more information.