Ridgetop Group Inc
ENGINEERING INNOVATION

RIDGETOP GROUP

Semiconductor Catalog

Comprehensive and effective

IP cores, software, and tools

- ✓ **F**unctionality: InstaCell™ Mixed-Signal Library
- ✓ **Y**ield Enhancement: nanoDFM™, including PDKChek® and YieldMaxx®
- ✓ **R**eliability: Sentinel Silicon™, ProChek™, and Q-Star Test™
- ✓ **E**ngineering Services

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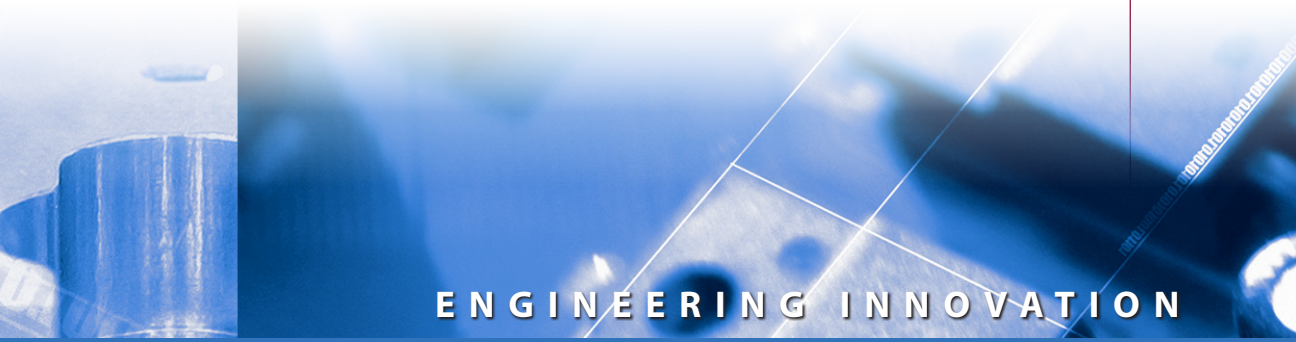
Part Number: RGFYRE Rev061714

Table of Contents



About Ridgetop Group

Ridgetop Group, based in Tucson, Arizona, is a highly specialized provider of custom analog test structures and process verification tools that support application-specific integrated circuit (ASIC) designers and semiconductor manufacturers. We provide state-of-the-art analog/mixed-signal InstaCell™ IP, especially for data converters and similar high performance devices. Our products provide many advantages, including fast and accurate access to process variation across die or wafer, improved IC design for manufacturability (DFM), monitoring of process drifts, and verification of specific model parameters that are critical to a design. Ridgetop's experience base covers IC designs across a broad range of technology nodes on various silicon processes for environmental conditions that range from mild to severe. Our staff members have impressive credentials and experience from leading firms such as IBM, Honeywell, Intel, BAE Systems, and Texas Instruments.

Overview

Since 2000, Ridgetop has provided customers with the very best products and services in semiconductor intellectual property (IP). This IP is in a number of areas that collectively we call Semiconductor FYRE, for functionality, yield, reliability, and engineering services.

FUNCTIONALITY

The **InstaCell™** library of analog and mixed-signal IP is a collection of blocks to accelerate your design process with circuitry of exceptional performance and value. Blocks range from complete analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to essential building blocks such as bandgap references and amplifiers.

InstaBIST™ is available for on-chip testing of ADCs.

Many of these blocks have been fabricated and fully tested, with silicon validation reports (SVRs) available.

YIELD IMPROVEMENT

PDKChek® is a library of patented die-level process monitors (DLPMs) that measure critical process mismatch parameters – threshold voltage (V_T) shift, capacitance, resistance, On current (I(on)) – so you can know when variation in your foundry's fabrication process is affecting your product performance.

YieldMaxx® is a convenient software tool for visualizing the mismatch data across single die, wafers, and lots.

RELIABILITY

The **ProChek™** semiconductor process characterization system is a powerful combination of reliability and characterization test IP available for virtually any DSM process, and a comprehensive yet compact benchtop test system. The benchtop induces semiconductor stress (voltage and temperature) via control structures on a test coupon, and measures degradation effects from negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), time-dependent dielectric breakdown (TDDB), hot carrier (HC) damage, electromigration, stress migration, and more. Radiation effects can also be measured.

The **Sentinel Silicon™** prognostic library includes die-level cores that can detect and notify you of impending failures due to deep submicron (DSM) semiconductor

effects and radiation degradation. The cores are co-located within your ICs and are able to provide remaining useful life (RUL) and state-of-health (SOH) metrics.

Q-Star Test™ is a line of precision current measurement instruments and modules and IP cores. The Q-Star modules are used for semiconductor characterization, verification, and test, and are optimized for I_{DDX} measurements. Q-Star IP can be integrated into a chip for the ultimate current measurement performance and convenience.

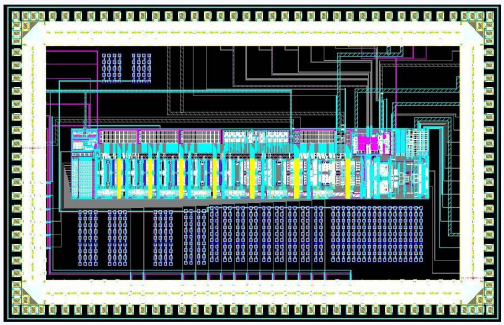
ENGINEERING SERVICES

Ridgetop Group provides a wide range of design services to help you move your IC ideas to reality. For example, we:

- Customize InstaCell IP blocks and design new ones to suit your specific needs.
- Design and validate part or all of a custom analog and mixed-signal ASIC using a complete tool chain from Cadence or others.
- Build a radiation-hardened ASIC from scratch or harden an existing ASIC design.
- Work with fabrication, packaging, assembly, and test houses to ensure the performance, quality, and reliability of the ASICs we design for you.
- Consult on design and test techniques to help you create circuits that are reliable and robust enough to withstand even the harshest environments, tuned to provide the highest level of analog/mixed-signal performance, and optimized for highly effective yet low-cost test and characterization.

This Semiconductor FYRE IP Catalog contains information helpful to the system-on-chip (SoC) designer in selecting modules for use in advanced designs.

If a particular analog or mixed-signal block does not appear in this catalog, please contact us as we may have other modules available or might be able to provide a custom design for you.



GDSII image of single-channel ADC that Ridgetop designed for a client

FYRE

InstaCell Library of Analog/ Mixed-Signal Design Cores

InstaCell is a library of high performance analog and mixed-signal IP blocks to help you accelerate your SoC design flow. Ridgetop Group provides IP blocks for state-of-the-art analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to the building blocks necessary to build these and other complex circuitry. Many of the InstaCell cores are radiation-hardened.

The DACs and Other IP tables (this page) and the ADCs (following two pages) summarize the InstaCell cores that are currently available.

Digital-to-Analog Converters (DACs)

Part #	Resolution	Key Specs	Foundry	Process	Sample Rate
DAC-RG8200	7 bits	Low power, wide supply range, output to positive rail	X-FAB XC06	600 nm CMOS	200 KS/s
DAC-RG16100	16 bits	Second-order digital delta-sigma modulator Area 0.8 mm^2	TSMC	0.25 µ	100 KS/s

Other InstaCell Analog & Mixed-Signal Design Blocks

Part #	Type	Key Specs	Foundry	Process
BGR 130A	Bandgap reference	0.8 to 1.3 VDD	IBM 8RF	130 nm CMOS
BGR 130B	Bandgap reference	0.6 V output	IBM 8RF	130 nm CMOS
Cascode 130	TBD	TBD	IBM 8RF	130 nm CMOS
BGR 600	Bandgap reference	Low power, wide supply range	X-FAB XC06	0.6 µm CMOS
Comparator 600	Comparator	Ultra low power, wide supply range	X-FAB XC06	0.6 µm CMOS
THA 130	Track-and-hold amplifier	Track-and-hold amplifier Input speed to 4 GHz	IBM 8HP	130 nm SiGe
Clock 130	Non-overlapping clock	Input speed to 4 GHz	IBM 8HP	130 nm SiGe

Analog-to-Digital Converters

Part #	RGADC-18B-500K-RH	RGADC-16B-400K	RGADC-14B-30M	RGADC-14B-40M
Topology	SAR	SAR	Pipeline	Pipeline
Resolution (bits)	18	16	14	14
Sampling speed (MSPS)	0.5	0.4	30	40
Analog bandwidth (MHz)	1	1	100	100
INL (bit)	1.5	1.5	±1.5	<2
DNL (bit)	1.0	1.0	±0.5	<2
THD	-112 dB	-100 dB	TBD	-65 dB
ENOB target	16 bits	14 bits	12 bits	10 bits
Latency (# of clock cycles)	20	18	TBD	7
Temp. range (°C)	0 to 70	0 to 70	-50 to 70	0 to 70
Input voltage range	2.5	2.5	±1	2
Power supply (volts)	3.3	3.3	+1.8/+3.3	3.3
Power (mW)	100	90	50	120
Radiation hardening (TID) (krad)	100	NA	NA	NA
Radiation hardening (SEL) (MeV-cm^2/mg)	NA	NA	NA	NA
Process	SiGe	CMOS	CMOS	CMOS
Foundry	IBM 130 nm	TSMC 180 nm	ONC18	TSMC 180 nm
Silicon Status	Designed	Designed	Taped out, Pre-silicon	Silicon proven

Analog-to-Digital Converters

Part #	RGADC-12B-40M-RH	RGADC-12B-100KX16	RGADC-10B-04M	RGADC-16B-30M-RH
Topology	Pipeline	Sigma Delta	Pipeline	Pipeline
Resolution (bits)	12	12	10	16
Sampling speed (MSPS)	40	26	4	30
Analog bandwidth (MHz)	50	0.1	10	100
INL (bit)	<1.5	<1.5	1.0	±5
DNL (bit)	±0.95	<1.0	0.5	±0.5
THD	-62 dB	-72 dB	-65 dB	TBD
ENOB target	11 bits	11.5 bits	10.2	12.2 bits
Latency (# of clock cycles)	3	256	7	TBD
Temp. Range (°C)	0 to 70	-40 to 85	0 to 70	-50 to 70
Input Voltage Range	0.2 to 1.0	2.5	4 Vpp Diff	±1
Power Supply (Volts)	1.2	3.3	3.3	+1.8/+3.3
Power (mW)	22.5 (9 in sleep mode)	<20	15	65
Radiation Hardening (TID) (krad)	>3500	NA	NA	100
Radiation Hardening (SEL) (MeV-cm^2/mg)	>120	NA	NA	100
Process	Thin-oxide 130 nm SiGe	CMOS	CMOS	CMOS
Foundry	IBM 130 nm	X-FAB 350 nm	TSMC 250 nm	ONC18
Silicon Status	Taped out, Pre-silicon	Silicon proven	Silicon proven	Designed

InstaBIST

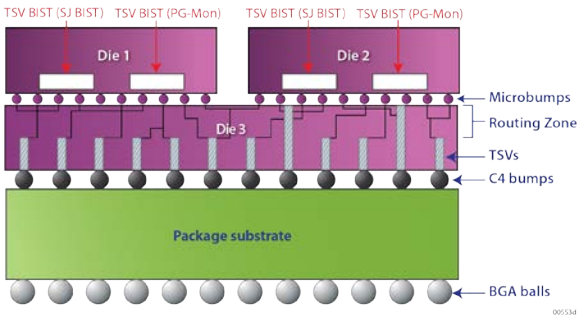
InstaBIST includes ADC BIST for on-chip self-test of high performance analog-to-digital converters, SJ BIST for testing of ball grid array (BGA) packages, and TSV BIST.

InstaBIST Products

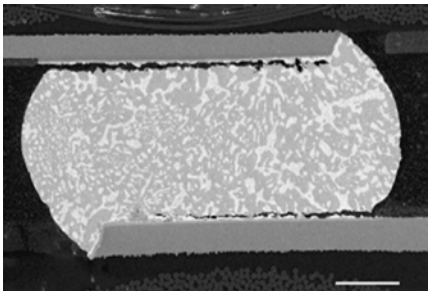
Product Name	Application	Description
RGADCBIST	Built-in self-test for analog-digital converters	Digitally invoked via the standard scan bus Interface IEEE 1149.1 (JTAG)
SJ BIST	BGA package to board interconnects reliability monitoring	Prognostic support Visualization software tool available
TSV BIST	2.5D ICs and 3D ICs	Ensures reliability of 2.5D and 3D IC components

TSV BIST

TSV BIST consists of tiny monitors, embedded into the 2.5D IC and 3D IC chip stacks, that can detect degradation in the chip-to-chip interconnections, identify intermittencies, and ultimately warn of impending interconnect failure – before the failure actually occurs.



TSV BIST reliability monitors embedded in stacked die in a 3D IC package



SJ BIST detects intermittents with many causes, including a cracked solder joint on the verge of fracturing, as shown above

nanoDFM Yield Enhancement IP and Software

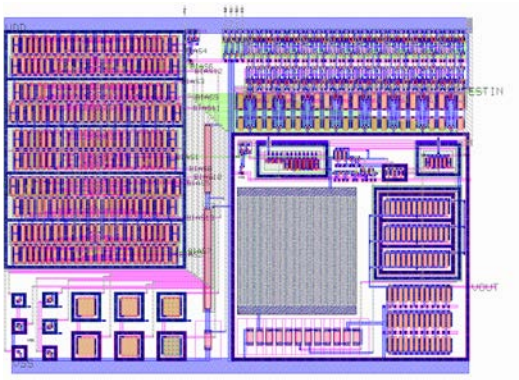
nanoDFM (nano Design-for-Manufacturing) is designed to help you maximize yield with foundry-independent IP blocks and software. PDKChek is a library of *in situ* IP cores that measure key process mismatch parameters, and YieldMaxx is a software program that provides visualization of results from PDKChek and other yield monitors. All can work in concert to provide the yield improvements that you seek.

PDKChek Die-Level Process Monitor (DLPM)

PDKChek is a library of patented die-level process monitors (DLPMs) that measure critical process mismatch parameters such as:

- Threshold voltage (V_T) shift
- Capacitance
- Resistance
- $I_{(ON)}$ (On current)

This enables you to know when variation in your foundry's fabrication process is affecting your product performance.



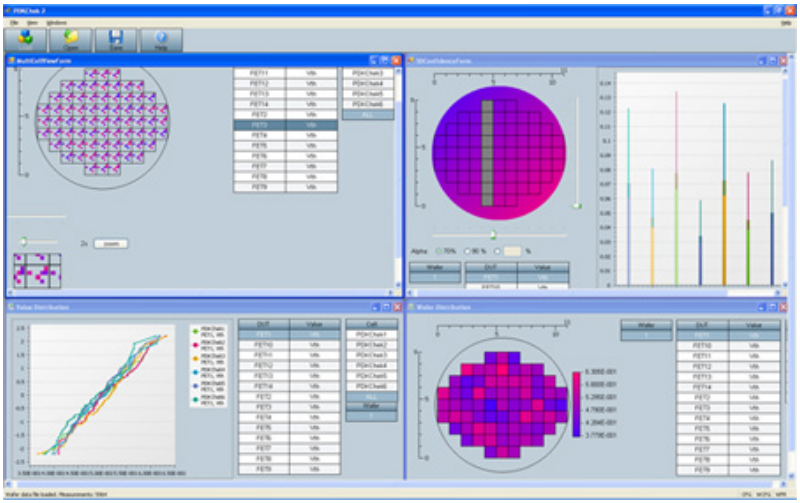
GDSII layout of PDKChek DLPM

Since PDKChek is packaged as a complete library, you receive a license for all available monitor cells for detecting process mismatch.

PDKChek works well with YieldMaxx for displaying measured results.

YieldMaxx DLPM Visualization Tool

YieldMaxx is a convenient software tool for visualizing the mismatch data across single die, wafers, and lots. YieldMaxx is delivered as a PC-based package and is preconfigured to accept data collected from PDKChek die-level process monitors and display the results in easily understood graphical form so you can quickly spot variation trends that may be adversely affecting yield of your designs at your foundries.



YieldMaxx graphical utility

Semiconductor Reliability Characterization Products

Ridgetop has state-of-the-art reliability characterization and monitoring tools capable of measuring and reporting on the most pernicious degradation effects known to exist in today's deep submicron (DSM) fabrication processes. If you are designing and building ICs where reliability is a primary concern, Sentinel Silicon, ProChek, and Q-Star Test products are essential for you to rest assured that your chips are continuing to perform as they should.

ProChek

Ridgetop Group's ProChek is an innovative system to qualify the performance and characterize the intrinsic reliability of deep submicron nanotechnology CMOS processes for microelectronics applications. ProChek is designed to provide fast and reliable measurement of critical electrical performance parameters. Subtle variations in these parameters can have significant adverse impact on the yield and performance of chips manufactured with modern semiconductor processes. ProChek also accelerates the process of gathering data concerning common degradation effects. These effects limit the lifetime of chips manufactured with all process nodes and some are exacerbated as feature sizes shrink. The ProChek methodology may be applied to both packaged chips and at wafer probe.

ProChek resources support measurement of many critical semiconductor wear-out mechanisms:

- Negative and positive bias temperature instability (NBTI, PBTI), including "fast" NBTI/PBTI
- Time-dependent dielectric breakdown (TDDB)
- Hot carrier (HC) damage
- Electromigration (EM) and stress migration (SM)
- Total ionizing dose (TID) radiation

ProChek benchtop test system

ProChek systems comprise four related components:

- Test coupons that contain test structures and Ridgetop test control IP for qualification and reliability characterization of the fabrication process(es) of your choice
- Benchtop instrument to control the voltage and temperature stresses applied to your test structures and to measure the results
- Test interface card to connect the benchtop instrument to the packaged test chip or to test chips residing on a wafer
- Host controller software running on a standard windows PC to support a wide range of built-in or customized semiconductor characterization and analysis procedures

The test coupon incorporates multiple arrays of test structures and an on-chip switching matrix to access, control, and observe the behavior of these test structures as they are stressed in parallel and measured individually. Depending on your needs, the test coupon may be:

(1) integrated on a single chip to maximize precision and test throughput

(2) divided across a test supervisor IC (TSIC) from a well-qualified process and one or more test chips (DUT IC) from the target process

(3) a board-level interface to traditional test structures through a wafer probe card or package assembly

ProChek reduces or even eliminates the need for expensive test equipment in fabrication process characterization. Testing is performed using multiple precision stress-and-measurement instruments embedded in the powerful yet compact benchtop system. The ProChek benchtop system and the host software are universal and can be used with different types of test coupons across different processes and fabrication runs. For even greater test acceleration, multiple ProChek benchtop systems may operate in parallel, controlled by a single host PC. The tight integration between the ProChek test coupon and the benchtop system enables an intuitive software interface so that programming using either pre-defined or user-specified test scenarios is quick and straightforward.

Because the integrated and TSIC/DUT IC test coupons can also incorporate on-chip heaters to rapidly elevate the temperature of selected test structures to over 300 °C (and a Peltier device

may also be controlled by ProChek), temperature-dependent effects are measured without the use of an oven. Regardless of the selected methodology, ProChek can dramatically lower the overall test cost and quickly deliver a large database of test results for statistical analysis.

ProChek is designed to deliver the essential process-level characterization data to both the fabless IC vendor and the foundry. Fabless manufacturers and ASIC designers know that their foundry cannot always supply them with all the device-level characterization data they need to maximize IC performance, yield, and reliability. Foundries and integrated device manufacturers (IDMs) need to measure and monitor each fabrication process to ensure that any drift or excessive variations are quickly understood and addressed. For companies and organizations where electronic reliability and lifetime performance is of paramount concern, characterization of IC manufacturing processes is a must.

For a complete description of the ProChek system, see the ProChek product brief at http://www.ridgetopgroup.com/doc/pb/PB_RGPCK-ProChek.pdf.

Sentinel Silicon

The Sentinel Silicon prognostic library comprises several die-level cores that can detect and notify you of impending failures due to DSM semiconductor effects and radiation degradation. The cores are co-located within your ICs and are able to provide remaining useful life (RUL) and state of health (SOH) metrics.

The tables below describe available Sentinel Silicon prognostic monitors.

Sentinel Silicon	
RGEM	Electromigration
RGNBTI	NBTI Prognostic Cell
RGPBTI	Positive Bias Temperature Instability
RGTDDB	TDDB Prognostic Cell
RGHCI	HCI Prognostic Cell

Sentinel Silicon	
RGRCFX	Field Oxide Prognostic Cell
RGSM	Stress Migration
RGRCVT	RadV$_T$ Prognostic Cell Rad-hard threshold voltage

Microinstruments

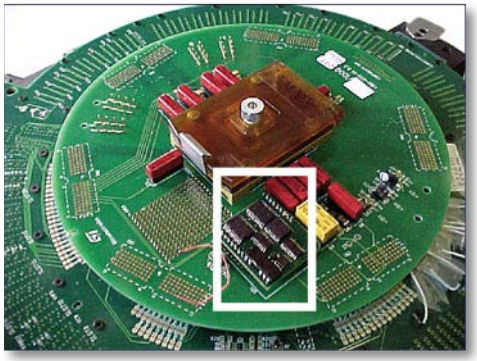
Q-Star Test (I_{DDX} Measurements)

Q-Star Test is a line of precision current measurement instruments that can determine whether your circuit is operating within acceptable bounds. Q-Star includes external modules that you affix to a test board to measure current for test applications such as I_{DDQ}, I_{DDS}, and I_{DDT} that can quickly and economically ascertain the quality of an IC. (For more information about Q-Star test modules, visit http://ridgetopgroup.com/products/semiconductor/QStarTest.php)

In addition, Q-Star provides IP in the form of Built-in Current Sensors (BICS). These on-chip monitors can perform the same functions as the off-chip modules (for example, I_{DDQ} testing) and can also be used for other applications, such as interconnection reliability monitoring in complex packages, such as flip-chip and 2.5D/3D ICs.

With over 800 installations at more than 50 semiconductor firms, Q-Star is a proven performer.

Q-Star Test	
BICMON	Full-featured built-in CMOS I_{DDQ} monitor core
TMON	Full-featured built-in CMOS I_{DDT} monitor core
PGMON	Built-in CMOS monitor core for IC connection verification



Q-Star precision I_{DDQ} instrument on ATE test head

IC Design Services

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- Customize InstaCell IP blocks and design new ones to suit your specific needs.
- Design and validate part or all of a custom analog and mixed-signal ASIC using a complete tool chain from Cadence or others.
- Build a radiation-hardened ASIC from scratch or harden an existing ASIC design.
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- Consult on design and test techniques to help you create circuits that are reliable and robust enough to withstand even the harshest environments, tuned to provide the highest level of analog/mixed-signal performance, and optimized for highly effective yet low-cost test and characterization.

Locations and Distribution Centers

Need modified or custom design?
Contact Ridgetop at +1 520 742 3300 to discuss your ideal solution!

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Worldwide Locations

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www.ridgetopgroup.com