### **IC Die-Level Monitoring Solutions**

#### **Ridgetop's Independent Die-Level Fab Process Monitoring Tools**

The semiconductor industry is shifting to a pure-play foundry model, and fabless integrated circuit designers rely on the accuracy of the Process Design Kit (PDK) that the foundries provide them.

"If data from the foundry are wrong, weeks can be wasted debugging ICs that were built with a process departing from the PDK."

But the PDK shares a limited amount of process information and is not made to fit every application. The foundry-supplied data may be obsolete, incomplete, or unavailable for specific transistors.

## CALL NOW TO SEE HOW WE CAN SAVE YOU TIME AND MONEY 520-742-3300

At Ridgetop Group, we develop families of intelligent, design-for-manufacturing tools covering the entire semiconductor development lifecycle. Our nanoDFM technologies provide techniques to improve the yield, design processes, and reliability of emerging nano-level processes for fabless and fab manufacturers.

These solutions are part of a suite of prognostic tools covering electronic devices from in-situ test structures on silicon to asset tracking software tools that manage across the globe.

## Breakthroughs for Fabless Semiconductor Designers

Ridgetop provides in-situ measurement solutions for IC, board, and modules used in critical systems. When you can monitor key parameter variation and performance degradation, you can take corrective or preventive action much faster and more easily.

### Why Do I Need Ridgetop Die-Level Test Structures?

Features	Advantages	Benefits
Independent in-situ monitor for precise measurement of $\Delta V_{rr} \Delta R$ , and $\Delta C$ (more features to follow)	Patented and independent means to evaluate mismatch of transistors	<ul> <li>Evaluate foundry performance</li> <li>Determine if problem is fab- or design-related</li> </ul>
"Baseline" foundry mismatch parameters	Independent and unbiased assess- ment for your specific transistor types	<ul> <li>Allows ongoing assessment of key performance indicators</li> <li>Supports foundry-to-foundry comparisons for best price/performance</li> </ul>
Small and unobtrusive design	Allows placement on the die where matching measurements are critical	Die-based location permits ongoing evaluation, unlike scribe-line approaches
Silicon-proven design built on decades of experience	Removes uncer- tainty for advanced design	Saves time and money

# Ridgetop Group Inc



#### **Changing Technology**

- Smaller IC geometries are leading to shorter lifetimes.
- Gate oxide thicknesses are very thin.
- Voltage supply is not scaling with dimensions.
- Wear-out mechanisms are emerging.
- Process-related variables are varying widely.

#### IC and Semiconductor IP Division

Diagnostic and prognostic products and tools designed for • nanoDFM™ integrated circuit fabrication and operation

- InstaCell™
- InstaBIST™
- Sentinel Silicon™
- Design Services



#### **Electronics Prognostic Division**

Prognostic products designed for use at the component level On-Board Sensors up through network management, using dedicated software • SJ BIST® and analysis tools

- RingDown™
- Sentinel Silicon Library™

#### Prognostic Health Management (PHM) Software (Sentinel Software™)

- Sentinel PHMPro®
- Sentinel Network<sup>™</sup>
- Sentinel Harness™

#### **On-Chip Sensors**

#### Sentinel Silicon<sup>™</sup> Library of Integrated Circuit Sensors

Sentinel Silicon acts as an early-warning sentinel of upcoming fault conditions as part of a Built-In Self-Test (BIST) in the host circuit. Sentinel Silicon measures the following aging-related degradation mechanisms: Hot Carrier Damage, Gate Oxide Failure (TDDB effect), Ionizing Radiation (Leakage and VT Shift), and Negative Bias Temperature Instability (NBTI).

#### **RingDown**<sup>™</sup>**Power System Prognostics**

Ringdown's non-intrusive health monitor provides advanced prognostic capability for power supplies and power actuator drivers, which can be the weakest link in an electronic device or system. A stand-alone solution, it provides detection and early warning of faults prior to performance degradation.

#### Solder Joint BIST™ (Built-In Self-Test)

Solder Joint BIST is a patented technology that detects real-time intermittent faults in operational FPGAs. Cracks, fractures, and other solder ball defects occur at the FPGA/BGA interface and were particularly difficult to detect before the SJ BIST innovation.

Ridgetop Group may from time to time make changes to the products or specifications contained herein without notice. The Ridgetop Group nanoDFM" technologies and PDKChek" are covered by U.S. patent 7,239,163 and other issued and pending patents



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