

# 16-bit DAC, 100 KS/s TSMC 250 nm IP Core

Semiconductor IP



## Industry-Standard, High-Performance DAC Technology

- 16 bits of resolution (14-bit accuracy)
- 100 KS/s sampling rate
- Second-order digital delta-sigma modulator
- TSMC 250 nm mixed-signal process
- 3.0 to 3.6 V analog supply voltage
- 2.25 to 2.75 V digital supply voltage
- Area 0.8 mm<sup>2</sup>
- Signal-to-noise: 94 dB at 50 kHz
- Signal-to-noise and distortion: 92 dB at 50 kHz input
- Includes complimentary license of patented PDKChek<sup>®</sup> die-level process monitor yield improvement solution

## General Description

Ridgetop's Audio DAC uses delta-sigma architecture. As shown in Figure 1, the DAC uses a digital interpolation filter, a digital second-order delta-sigma modulator, and a 32-tap analog reconstruction filter FIR. A fourth-order modulator is available to decrease oversampling ratio if the application requires. Applications for this core include audio commercial electronics, industrial control, and automotive. Table 1 gives the summary of DAC core specifications.

## Applications

- Consumer electronics
- Audio commercial electronics
- Hi-fi audio applications
- Industrial controls
- Automotive

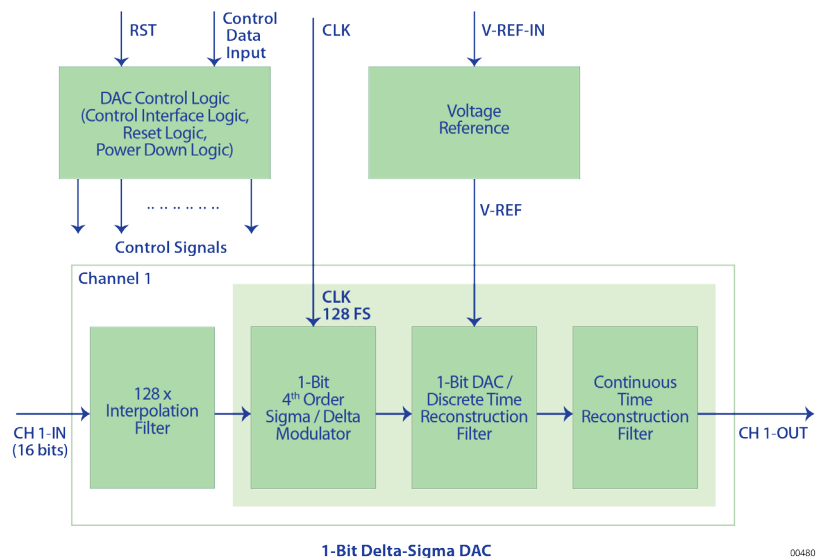


Figure 1: DAC design

**Table 1: Summary of DAC Core Specifications**

| PARAMETER                                   | SPECIFICATION  | NOTES |
|---|--|-------|
| Accuracy                                    | 16-bit resolution (14-bit accuracy)                        |       |
| Sampling rate                               | 100 KS/s   |       |
| Digital input data format                   | 16-bit parallel @ Fs (single-ended)                        |       |
| Sampling frequency (Fs)                     | 0 Hz to 100 kHz  |       |
| Digital input data frequency                | 45 kHz (max)   |       |
| System clock frequency                      | 25.6 MHz   | 1     |
| Analog supply voltage                       | 3.0 V (min), 3.3 V (typ), 3.6 V (max)                      |       |
| Analog supply current                       | ~10 mA (typ)   |       |
| Digital supply voltage                      | 2.25 V (min), 2.5 V (typ), 2.75 V (max)                    |       |
| Digital supply current                      | ~22 mA (typ)   |       |
| Temperature range                           | -40 to +125 °C   | 2     |
| Signal-to-noise ratio (SNR)                 | 94 dB  |       |
| Signal-to-noise-and-distortion ratio (SNDR) | 92 dB  |       |
| Offset error                                | ±30 mV (max)   |       |
| Differential nonlinearity (DNL)             | ±0.1 LSB (max)   |       |
| Integral nonlinearity (INL)                 | ±0.2 LSB (max)   |       |
| Reference voltage                           | 1.22 V   |       |
| Analog output voltage                       | 1.65 V ±1.0 V (single-ended)                               |       |
| Center voltage                              | 1.65 V   |       |
| Load impedance                              | 1 KΩ (min)   |       |
| NOTES                                       |  |       |
| 1   | Customer will supply 25.6 MHz clock signal to DAC IP block |       |
| 2   | Temperature may cause roll-off in specifications           |       |

Figure 2 shows a GDSII image of the DAC.

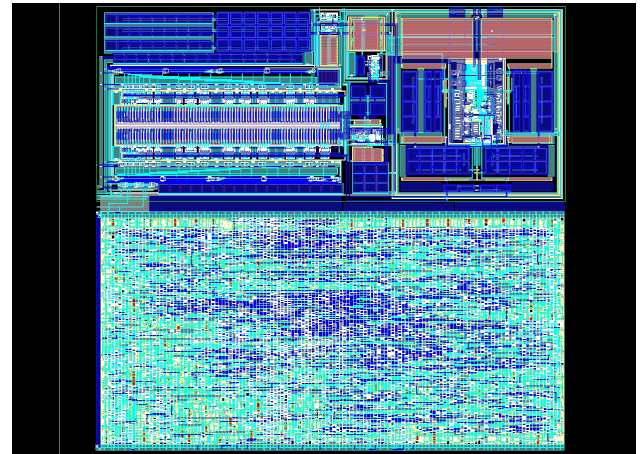


Figure 2: GDSII image of DAC layout

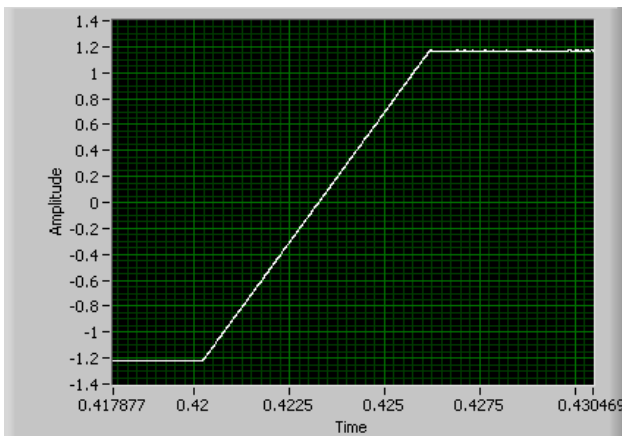


Figure 3: Waveform, 1 kHz, reduced amplitude, no load, sampling frequency 100 KS/s

In Figure 3, the reduced-amplitude, no-load peak-to-peak voltage was measured as 1.463 V, which compares favorably with an ideal peak-to-peak of 1.488 V (25 mV difference).

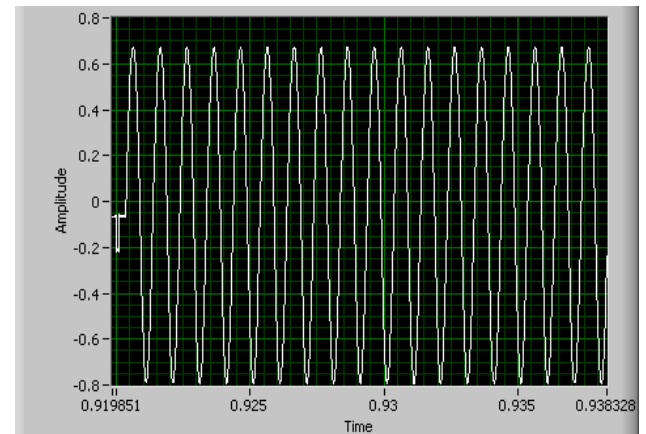


Figure 4: Waveform, linear ramp, 14-bit digital codes, full amplitude, no load, 100 KS/s

The waveform in Figure 4 shows that a linear ramp generated by small digital code increments is relatively distortion-free.

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### Corporate Headquarters

3580 West Ina Road  
Tucson, Arizona 85741 USA  
OFFICE +1 520 742 3300  
INFO@RIDGETOPGROUP.COM

### Worldwide Locations

Support and sales locations for Ridgetop Group Inc. exist in Germany, Belgium, Japan, China, and the United States.  
For office locations and contact information, please call the corporate headquarters or visit us on the web: [www.ridgetopgroup.com](http://www.ridgetopgroup.com)