ProChek™ Wafer-Level Semiconductor Process Characterization System

AS9100C
CERTIFIED QUALITY MANAGEMENT SYSTEM
*ISO9001:2008*
CERTIFICATE NO. 1107004

Integrated Circuit Fabrication Process Qualification and Reliability Analysis

- Complete device-level characterization system
- Compact platform for convenient interfacing with wafer-level test structures
- Built-in testing protocols for NBTI, PBTI, TDDB, HC, EM, SM
- User-programmable and configurable test conditions
- Makes "Fast NBTI/PBTI" measurements to observe annealing effects
- Available direct or cabled interface

- Independently verifies foundry PDK parameters
- Innovative optional test coupon architecture accelerates testing through highly parallel test methods
- Available on-chip heaters improve test throughput
- Reduces the need for expensive auxiliary test equipment
- Suitable for both new and qualified CMOS, SiGe, and SOI process nodes
- Supports large array of test structures for parallel testing

Product Description

Ridgetop Group's ProChek is an innovative system to qualify the performance and characterize the intrinsic reliability of deep submicron nanotechnology CMOS processes for microelectronics applications. ProChek is designed to provide fast and reliable measurement of critical electrical performance parameters. Subtle variations in these parameters can have significant adverse impact on the yield and performance of chips manufactured with modern semiconductor processes. ProChek dramatically reduces the cost of gathering wafer-level data concerning common degradation effects. These effects limit the lifetime of chips manufactured with all process nodes and some are exacerbated as feature sizes shrink. It can also perform faster than traditional wafer-level test methods through support for highly parallel test execution.

ProChek platform

ProChek reduces or even eliminates the need for expensive test equipment in fabrication process characterization. Testing is performed using multiple precision stress-and-measurement instruments embedded in a powerful yet compact unit which includes a graphical user interface setup and control application and results analysis tools. The ProChek platform and the host software are universal and can be used with different types of test chips across different processes and fabrication runs. The ProChek platform is extremely small (less than 14 cm x 17 cm x 4 cm, and weighs about 610 g) yet comprises instrumentation comparable to larger (and more expensive) rack-mounted equipment, making it a simple matter to move ProChek from a probe station in one lab or floor area to another, as needed.
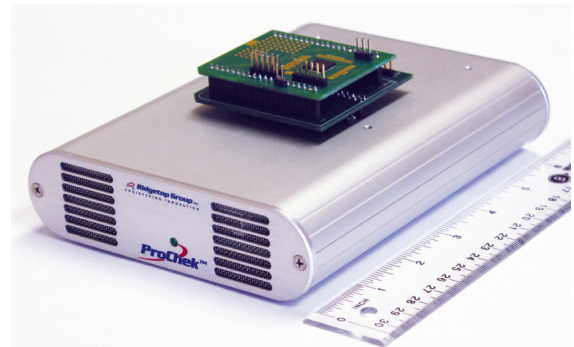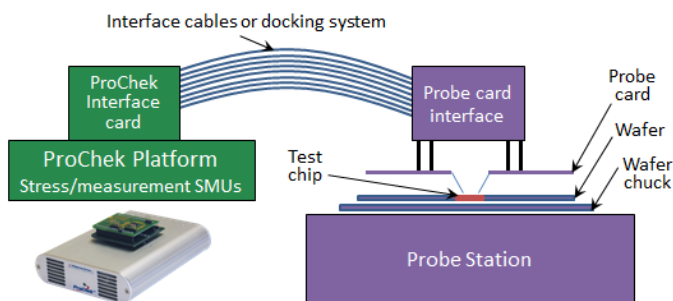
The ProChek platform can be connected to the wafer probe system either with cables or a direct docking system

You can choose to interface your wafer-based test structures directly to the ProChek platform or you can embed them within a customized test "coupon" which includes on-chip switches, control logic, and heaters. The interface from ProChek to the probe station consists of a test interface card mounted on the ProChek platform and connecting to the prober via a set of high quality cables or through a direct-dock system. Using a ProChek test coupon as the test chip on the wafer minimizes the signals required to be transmitted across the interface because a serial data stream is sent from the ProChek system to the test coupon, where decoding and selection logic is used to address specific devices-under-test (DUTs) on the test coupon. A standard test chip normally requires a separate interface signal for each

terminal of each DUT, and the address decoding occurs on the test interface card on the ProChek platform.

Whether you use your existing test structures or a ProChek test coupon, the tight integration across the instrumentation embedded in a single ProChek platform enables an intuitive software interface so that programming using either pre-defined or user-specified test scenarios is quick and straightforward. ProChek is equipped with accelerated stress test setups targeting reliability concerns such as negative and positive bias temperature instability (NBTI, PBTI), time-dependent dielectric breakdown (TDDB), hot carrier (HC) damage, electromigration (EM), and stress migration (SM). ProChek even supports "fast NBTI/PBTI" measurements, observing the sub-microsecond onset of annealing effects, because it can switch from stress to measurement mode without missing a beat.

Accuracy and Performance to Meet the Market's Needs

ProChek is designed to deliver the essential process-level characterization data to both the fabless IC vendor and the foundry. Fabless manufacturers and ASIC designers know that their foundry cannot always supply them with all the device-level characterization data they need to maximize IC performance, yield, and reliability. Foundries and integrated device manufacturers (IDMs) need to measure and monitor each fabrication process to ensure that any drift or excessive variations are quickly understood and addressed. For companies and organizations where electronic reliability and lifetime performance is of paramount concern, characterization of IC manufacturing processes is a must.

With its accurate instrumentation, portable hardware, flexible interface, and easy-to-use software, ProChek fits – literally and figuratively – into virtually any process-level characterization flow.

Optional ProChek Test Coupon for Further Test Optimization

With the innovative ProChek test coupon option, ProChek becomes even more cost-effective and time-efficient. Together the ProChek platform and test coupon comprise a comprehensive solution that delivers results for some of the most difficult device-level characterization tasks. The test coupon is manufactured using the target fabrication process and can contain multiple arrays of test structures to be characterized under various conditions. In addition to the test structures, the test coupon incorporates an on-chip switching matrix to access, control, and observe the behavior of these test structures as they are
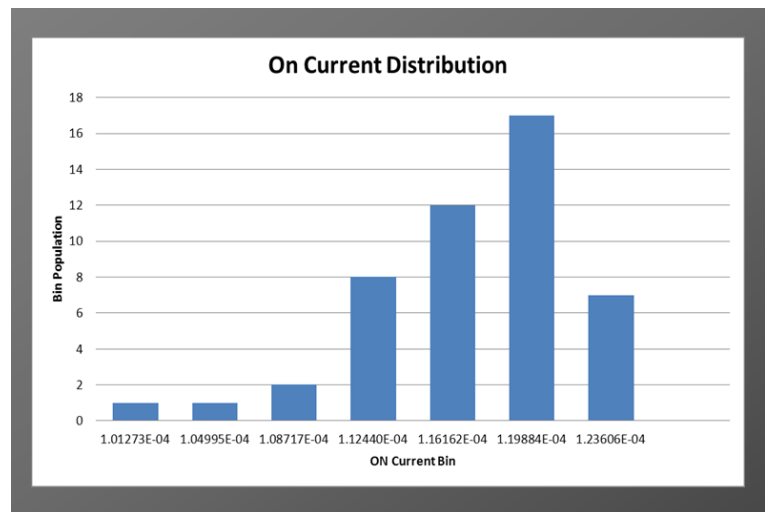
Distribution of On Current in 48 NFET DUTs on three ProChek test coupons

stressed in parallel and measured individually. Two test coupon configurations are available to meet different cost and performance targets:

(1) All the test coupon functionality is integrated on a single chip to maximize precision and test throughput; this approach minimizes the interfacing overhead since all the selection and switching mechanisms are on the test coupon itself, and also eliminates the need to use a heater wafer check if the ProChek heaters are used; and

(2) For characterization and qualification of newer processes, or for test chips without the embedded ProChek switching matrix, the device selection and addressing is performed on the test interface card mounted on the ProChek platform.

Regardless of the selected method, ProChek can dramatically lower the overall test cost and quickly deliver test results for statistical analysis.

Additional Information

Ridgetop offers technical support to assist customers at every step in the process. Our design and support team has extensive experience in CMOS and SiGe bipolar IC design semiconductor process technologies, and practical, results-oriented engineering. We assist customers with product and applications training, design and implementation of ProChek test coupons, test planning and execution, and other support services to ensure that the ProChek experience is beyond expectations.

Need modified or custom design? Contact Ridgetop at +1 520-742-3300 to discuss your ideal solution!

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