Ridgetop Group *Inc*

ENGINEERING INNOVATION

PDKChek® Independent Die-Level Monitor

Semiconductor IP

CERTIFIED QUALITY • ISO9001:2008 • AS9100C • CERTIFICATE No: 1107004 • MANAGEMENT SYSTEM

Industry-Standard, High-Performance, Process Design Kit (PDK) Technology

- Independently verifies PDK parameters
- Expedites problem resolution
- Resolves yield detractors
- Optimizes design margins
- Provides feedback for self-calibrating circuit
- Offers specific transistor selection
- Facilitates testing

- Includes complimentary licensed PDKChek die-level process monitor yield improvement solution
- Precise mismatch measurement sensors: threshold voltage, resistance, capacitance, and turn on/off current

- Extracts process-induced variance on die level
- Stand-alone measurement IP block, unobtrusive to host circuit
- Minimal area trade-off, low-power design
- Versatile functioning determines I(on) or I(off)

General Description

Fabless designers rely on the accuracy of the process design kit (PDK) supplied by the foundry in accounting for the statistical nature of the offset voltages. However, a foundry PDK does not exactly model all choices of devices. At process geometries of 130 nm and below, the designer requires a tool like PDKChek to accurately determine the relevant parameters for the specific devices used in the design (width and length choices). Figure 1 describes the PDKChek system-level implementation. The ΔV_T, ΔR, and ΔC sensors are available, and the inductance sensor is currently being tested.
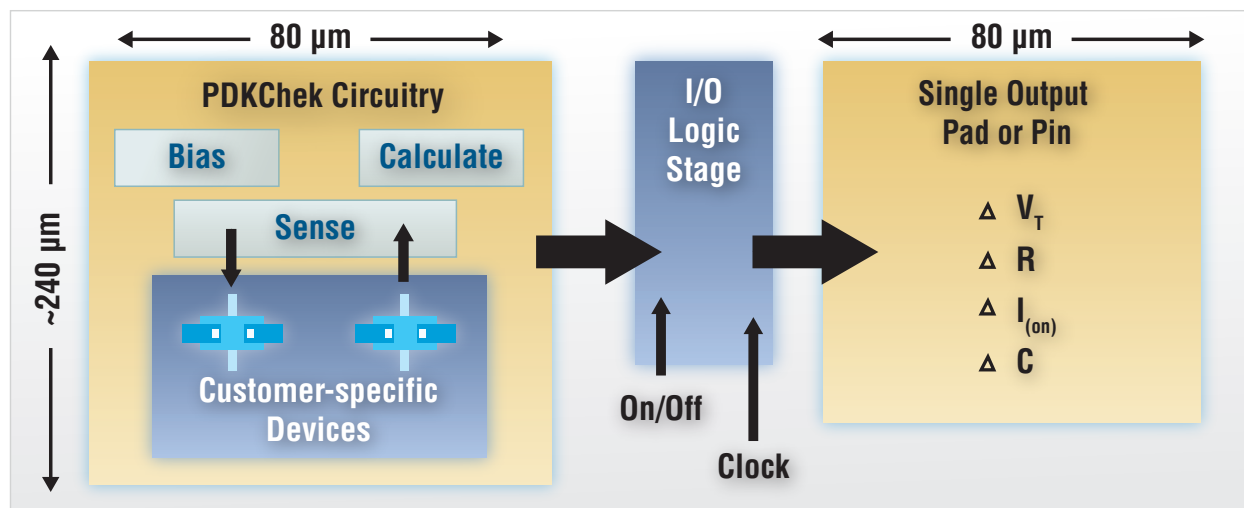

Figure 1: PDKChek system-level implementation

Matching performance is a key parameter for CMOS processing. Mismatch in transistor threshold voltage, resistance, and capacitance are dominant factors in IC performance. Mismatch in V_T can increase offset voltage, CMRR and poor performance. Differences in turn-on current in digital circuits produce timing errors, reduce design margins, and can impact yield. Process-related parameter variance is inversely proportional to transistor area and therefore becomes increasingly important as the dimensions of the transistors are reduced.

The influence of local process-related variations in device characteristics on electrical parameters of an IC is becoming a critical issue as device geometries and power supplies continue to decrease.

Ridgetop's PDKChek measures die-level process-induced variations, both random and systematic, in MOS transistor threshold voltage (V_T), resistance, capacitance, and turn on/off current. PDKChek is an unobtrusive, stand-alone, IP block designed to accurately and precisely measure the variation in parameters resulting from the randomness inherent in processing.

The PDKChek IP block provides circuit designers with independent verification data to improve the accuracy of process design margins, increase process yield, expedite problem resolution (design- or process-related), reduce design iterations (duration and frequency), and enable shorter time to market.

PDKChek allows for faster testing than traditional scribeline transistors. Testing can take place before or after packaging the die. Die-level testing takes advantage of test structures and bonding pads that are already present on the die, so there is no additional error introduced by the contact resistance of a probe station.

Technical Specifications

The process monitor is co-located on the same circuit as the host circuit, thus ensuring that the sample provides an accurate representation of the devices on the chip.

To calculate the statistical distribution of the parameter values, an array of the sensors can be employed as well as additional analytical circuitry. The total sample size is:

Sample Size = (# of dies) x (# cells per die)

This process monitor measurement provides statistical distributions of the parameters including any spatial and angular variation that may exist throughout the wafer.

The design is flexible and can be applied in several different ways, depending on the power and size constrictions of the ASIC. The most basic configuration consists of only the process monitor along with the associated control circuitry. This configuration results in the lowest possible power and area consumption.

An ADC can be added to the process monitor as an option in order to provide ease of testing. The tradeoff for adding the ADC is increased power consumption and size.

As an additional add-on when using an ADC, Ridgetop offers a JTAG interface to access the process monitor. This standard interface offers easy access to the process monitor through four pins and also allows access to any other parts of the ASIC if the design is integrated with the JTAG.

Accuracy

The PDKChek die-level process monitor measures the values of the parameter mismatch with 8-bit accuracy. Increased accuracy is available through the analog interface.

Interface

Ridgetop provides an optional JTAG (IEEE-1149.1) interface in the design of the process monitor. The JTAG interface is especially useful for applications where the number of pads on a chip are limited since JTAG allows interfacing to the process monitor through only four pins.

The JTAG interface is also useful if a digital interface does not already exist on the ASIC or if a digital interface is desired over an analog interface. It can also be interfaced to other portions of the ASIC in order to extract data unrelated to the process monitor. JTAG is a standard serial bus and uses five input/outputs for communication:

- TDI - Test Data In

- TDO - Test Data Out

- TCK - Test Clock

- TMS - Test Mode Select

- Reset (optional)

The JTAG logic accepts all required commands from a JTAG controller and can be expanded to accept optional commands.

Figure 2 illustrates the GDSII layout of the PDKChek die-level process monitor (DLPM).

Power Dissipation and Size Considerations

The power dissipation and size requirements for the process monitors are low (see Table 1). As additional process monitors are added to each die in order to increase the measurement sample size, the area and power dissipation increase. If optional components such as the DAC, ADC, and JTAG interface are added the power dissipation and size of the process monitors increase further.

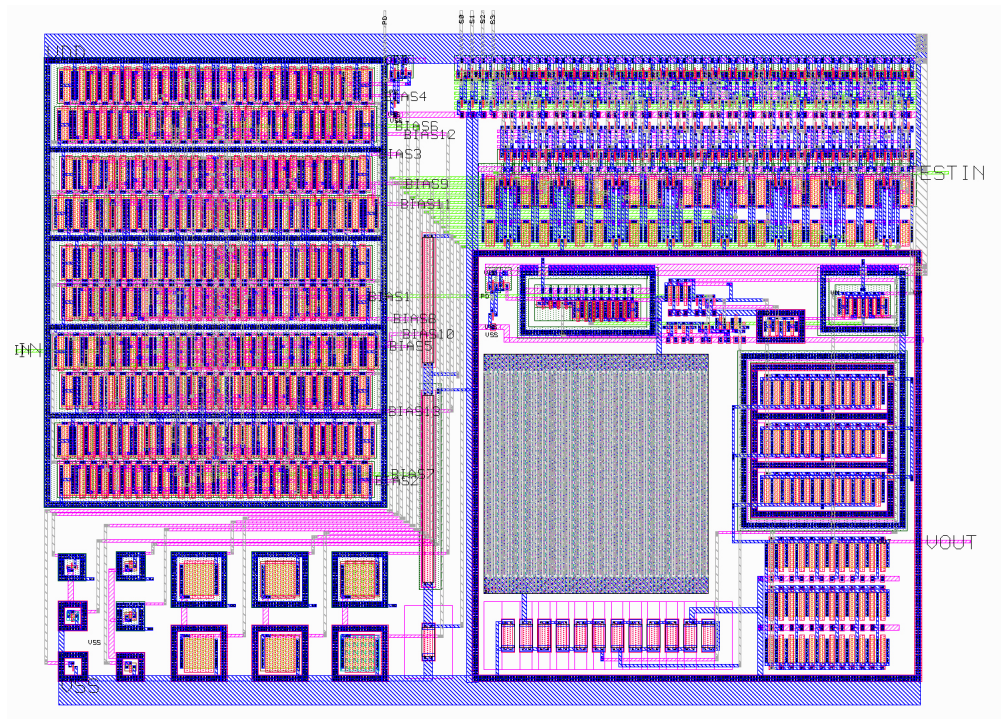Figure 2 shows the GDSII layout of the PDKChek DLPM.

Figure 2: GDSII layout of PDKChek die-level process monitor (DLPM)

Table 1: Size and Power Dissipation for Process Monitor

IC Integration Support

Ridgetop offers IC integration technical support to assist customers at every step in the process. Our design team has extensive experience in CMOS and Bipolar IC design semiconductor process technologies, and practical, results-oriented engineering.

Size and Power Dissipation for Process Monitor		
	For 90 nm technology:	
Sensor Cell	Power	Area
Threshold voltage	30 µW	80 x 60 µm
Resistance	30 µW	80 x 60 µm
Capacitance	50 µW	80 x 80 µm
Bandgap ref (if required)	150 µW	200 x 200 µm
ADC (if required)	50 mW	700 x 400 µm
JTAG interface (if required)	40 mW	700 x 400 µm

PDKChek is a registered trademark of Ridgetop Group Incorporated. Patent Issued.

Need modified or custom design? Contact Ridgetop at 520-742-3300 to discuss your ideal solution!

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