PGMON
Product Highlights

Built-in CMOS Monitor Core for IC Connection Verification

FEATURES

- Small Chip Area: 95x100µm² (0.35µm CMOS)
- Detection range: 1.5 – 4.0 Ω
- Maximum measurement rate: 20 kHz
- (Boundary) Scan Controllable (3 pins)
- No calibration needed
- Easily transferable to other CMOS processes

APPLICATIONS

- On-chip Power Connection Verification
- Wafer Sort Testing
- On-chip I/O Continuity Checks

DESCRIPTION

The PGMON is a non-invasive, highly reliable, (boundary) scan controllable on-chip CMOS current monitor and is applicable at SOC, board and system level. The purpose of the monitor the validation of power and ground connections. However, the PGMON can also be used for the verification of any Integrated Circuit Connection (ICC). ICCs in this context comprise on-chip connections as well as connections between an IC and its application substrate, including bonding and soldering. (e.g. when mounting an IC on a PCB, MCM, Flip-Chip, Chip Scale Packaging, SOP,…, or for IP units part of an SOC).

The PGMON is fully transparent to the circuit of which the connections are being monitored; it does not affect the operation nor the performance of the circuit of which the connections are verified. The particular design guarantees a proper detection, irrespective of local and global process parameter variations (as illustrated in figure 2) hereby avoiding the need for calibration. The circuit can be put in a power down mode.

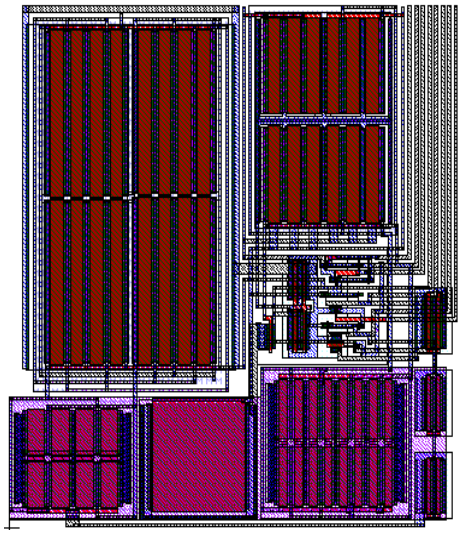

Figure 1. PGMON Core

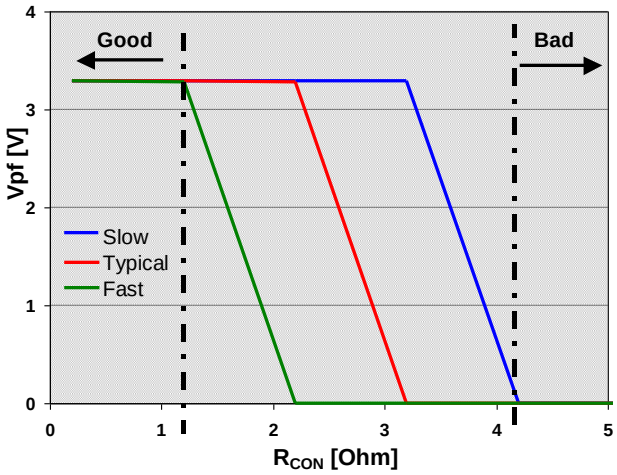

Figure 2. PGMON Operation

To characterise and validate the design concept an implementation was done using the Alcatel Microelectronics 0.35µm CMOS technology. The PGMON core is shown in figure 1, the core size for this technology is 95x100µm². The parameters listed in this document refer to that implementation, targeted for use in combination with 3.3V devices. However, the PGMON is not restricted to this technology and supply voltage. The design is easily transferable to other CMOS processes and voltages.

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TEST METHODOLOGY

The test methodology to verify power and ground connections using an on-chip monitor is based on detecting a (supply) current flowing between a bonding pad and its connection to the IC power supply distribution network. The detection mechanism makes use of the inherent resistances of the IC power distribution network (R_{CONx} and R_{PRx}), as illustrated in the figure 3.

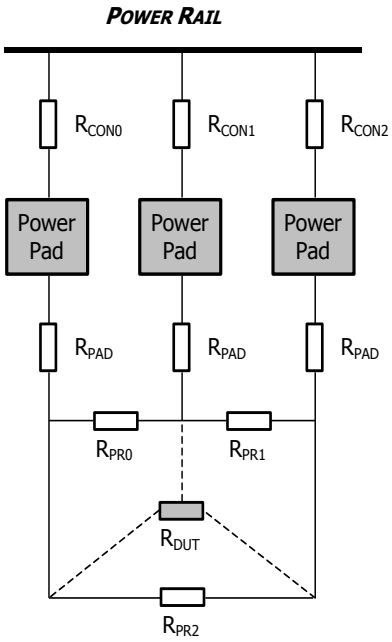

Figure 3. IC Power Distribution Network

To verify if a proper connection is present, either the current through the pad or through the supply ring can be observed. As all supply connections are connected in parallel, the test current will not solely be provided by the Pad Under Test (PUT). When the PUT connection is intact, most of the current will be drawn via the PUT causing a significant voltage drop across R_{PAD}. A small part of the test current will be drawn via the supply ring resulting in a small voltage drop across the adjacent ring segment resistors R_{PR}s. When the PUT connection is defective all current will be drawn via the resistor network resulting in a negligible voltage drop across R_{PAD} and a significant voltage drop on either or both of the adjoining R_{PR}. As such, a pass/fail decision can be made based on the voltage levels across R_{PAD} and/or the adjoining R_{PR} resistors of the PUT. Hence two types of monitors can be distinguished, a *pad monitor* and *a ring monitor*, as illustrated in Figure 5. The pad or ring monitors are placed respectively on the pad segment or the ring segment of the supply distribution network.

The test methodology to verify I/O connections is similar but simpler. As no distribution network is present, the test current is supplied solely by the Pad Under Test (PUT). When the PUT connection is intact, the test current flows via the PUT causing a significant voltage drop across R_{PAD}. When the PUT connection is defective, no current flows through the pad causing no voltage drop across R_{PAD}. As such, a pass/fail decision can be made based on the voltage levels across R_{PAD}, requiring only the use of *pad monitors*.

CIRCUIT DESCRIPTION

The figure below shows the block diagram of the V_{DD} pad monitor. The monitor can be seen as consisting of a current sensor, a sampling circuit, a voltage comparator and a controlled current sink. As the current drawn by the DUT varies from application to application and from state to state, a controlled current sink/source is added to each pad-ring connection to guarantee a steady current flow through the observed resistor during the measurement. The current sink/source connected to the Pad Under Test (PUT) is activated when a measurement is performed.

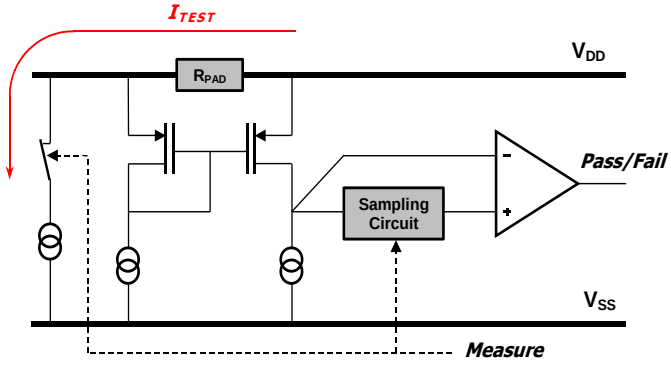

Figure 4. V_{DD} Monitor Block Schematic

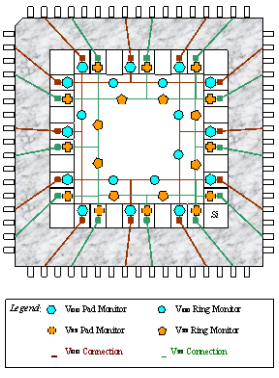

Figure 5. Possible Monitor Locations