

# Ridgetop Group, Inc.



**Ridgetop Group Facilities in Tucson, AZ**

- Arizona-based firm, founded in 2000, with focus on electronics for critical applications
- Two divisions: Semiconductor & Precision Instruments (SPI) and Advanced Diagnostics & Prognostics (ADP)
- Technology leader in precision test structures for QA and prognostic applications
- Wide range of commercial and government customers

- Worldwide nanotechnology R&D partners in industry and academia
- Foundation and focus in physics-of-failure for electronic systems



**Ridgetop Europe Facilities in Brugge, Belgium**



**Ridgetop Group** INC

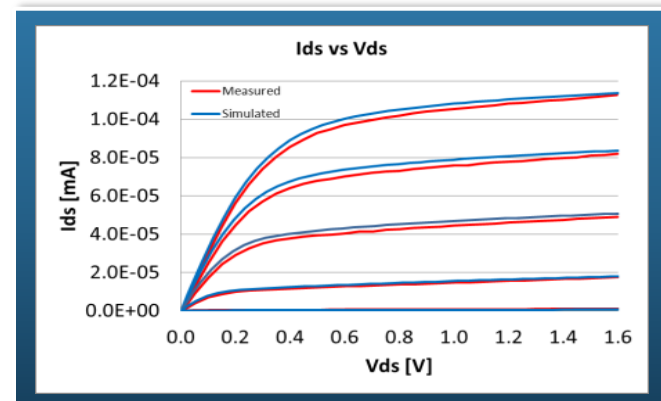
Engineering Innovation in Electronic Prognostics



## Semiconductor Process Qualification & Reliability Characterization System

# Foundry PDK May Not Be Sufficient

Reliability Concerns	Foundry PDK	ProChek
Variations Across Wafers & Lots		■
Application-specific effects (e.g., temperatures, radiation, biasing, specific geometries)		■
Physical fabrication effects (e.g., directional, wafer angle)		■
Random parameter fluctuation simulation data		■



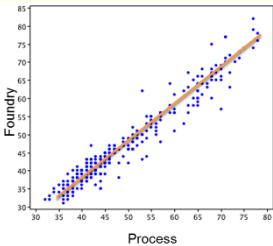
# Characterization Systems Should...



Deliver lots of data

- Quickly
- Accurately & repeatably
- For different devices
- For different operating conditions

Be inexpensive to own and operate



Allow for direct correlation across foundries and processes

Be easy to use



# What is ProChek?

An innovative low-cost technique to rapidly



characterize intrinsic process reliability and monitor process quality

## ProChek...

- Is a flexible & dedicated semiconductor qualification and reliability characterization system.
- Is based on a cost-effective bench-top instrument.
- Uses a specially designed test chip integrated with the bench-top instrument.
- Accelerates testing of semiconductor devices in volume.
- Puts key instrumentation on silicon to reduce cost, increase flexibility, improve capability, shrink the footprint.

ProChek reduces data collection from months to days



# ProChek Characteristics

Characterizes deep submicron (DSM) processes (bulk CMOS, SiGe, SOI) reliability and variability effects

## Test Coupon

- Low cost
- Easily ported
- Small as 1 mm x 1 mm area
- Easily controlled: Fully programmable test conditions cover DC and AC stress cases
- Highest throughput: Test time reduced from months to hours
  - Tests from hundreds to over a thousand devices
  - Local heaters elevate temperatures up to over 300 °C

## ECTC

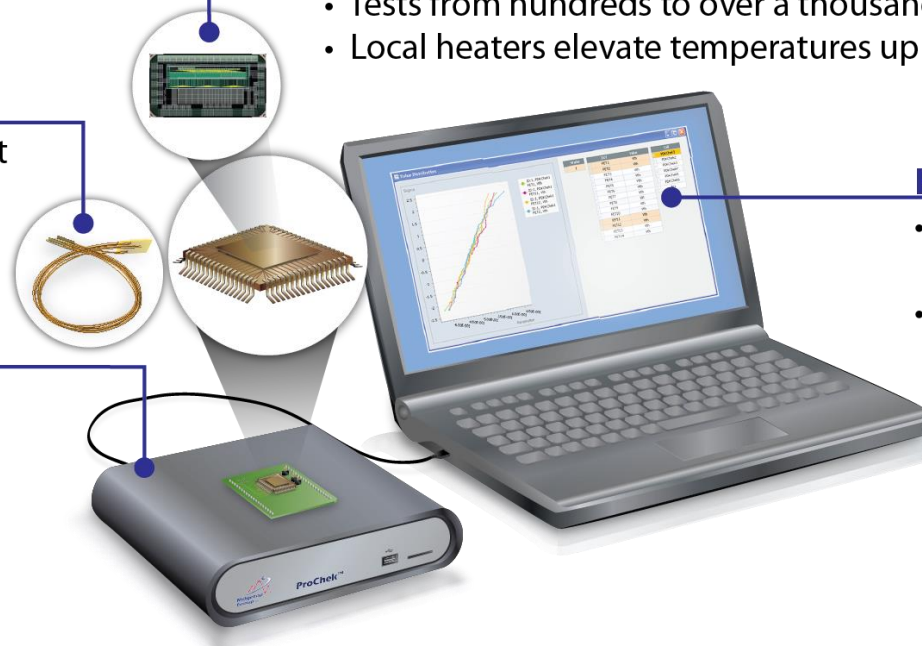
- Environmental chamber test cable for placing test card in environmental chamber (optional)

## Benchtop Tester

- Universal: Supports all test coupons
- Low cost: No “big iron” ATE or oven required
- Contains/controls all stress and measurement instruments

## Host Controller

- Easy-to-use software interface
- Local data processing

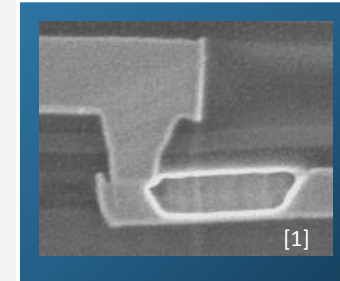


**Key ProChek Benefits: Accurate, Comprehensive, Fast, Affordable**

# ProChek Data Collection

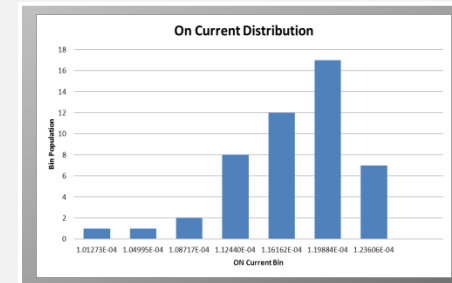
Major degradation effects and accelerated stress

- Negative Bias Temperature Instability (NBTI / Fast-NBTI)
- Positive Bias Temperature Instability (PBTI / Fast-PBTI)
- Time-Dependent Dielectric Breakdown (TDDB)
- Hot Carrier (HC) Damage
- Electromigration (EM)
- Stress Migration (SM)



Accelerated data collection

- Collection of data from multiple DUTs simultaneously
- DUT degradation is accelerated with electrical and thermal overstress
- Statistical analysis of collected data/results



[1] Ki-Don Lee, et al., "VIA PROCESSING EFFECTS ON ELECTROMIGRATION IN 65 NM TECHNOLOGY", 44th Annual International Reliability Physics Symposium, San Jose, 2006

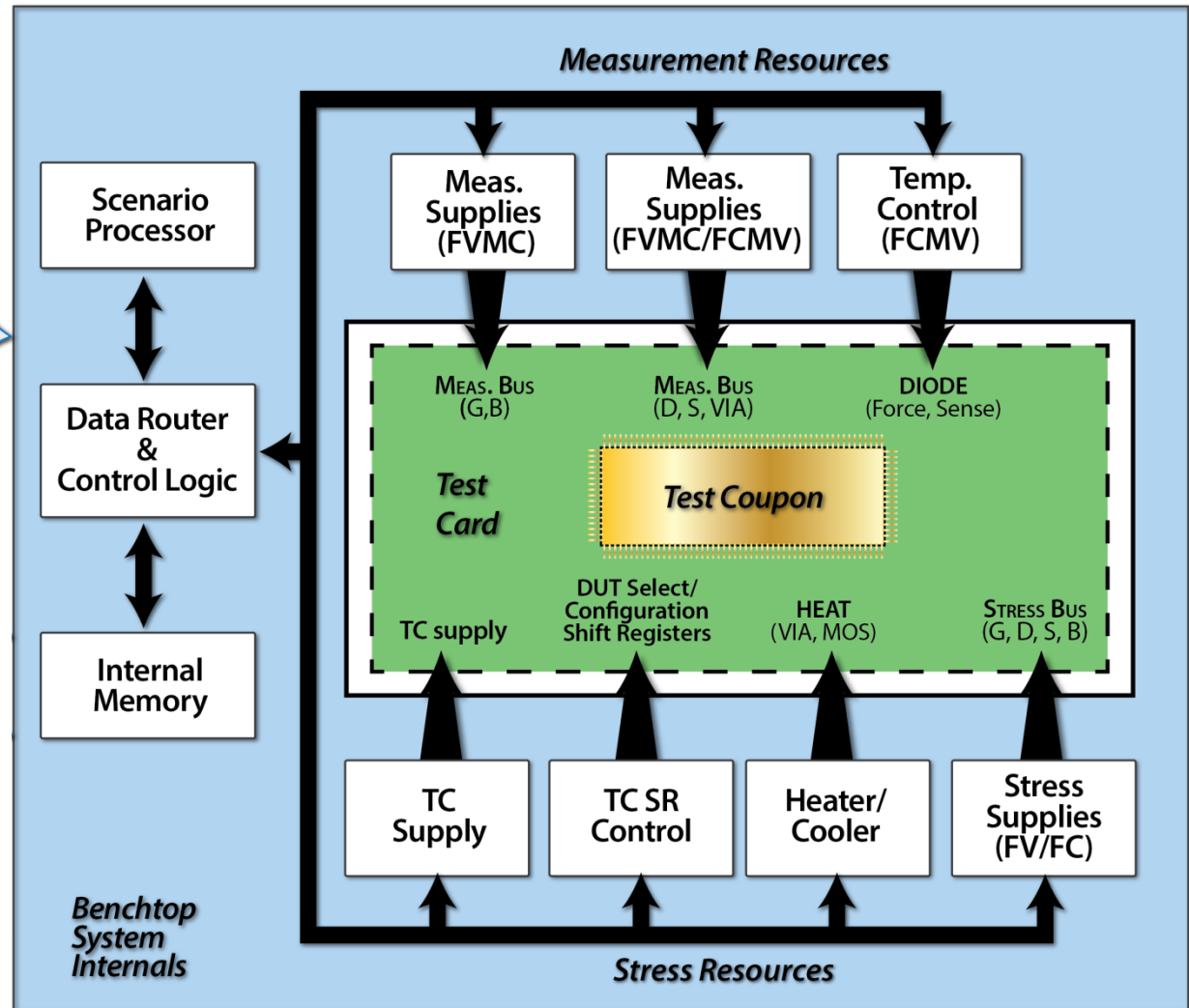
# ProChek Benchtop Tester Architecture



## Computer GUI

- » Test Setup & Control
- » Result Collection
- » Result Processing

USB 2.0



00425c



# Accelerated Testing

## Combining Thermal and Electrical Overstress

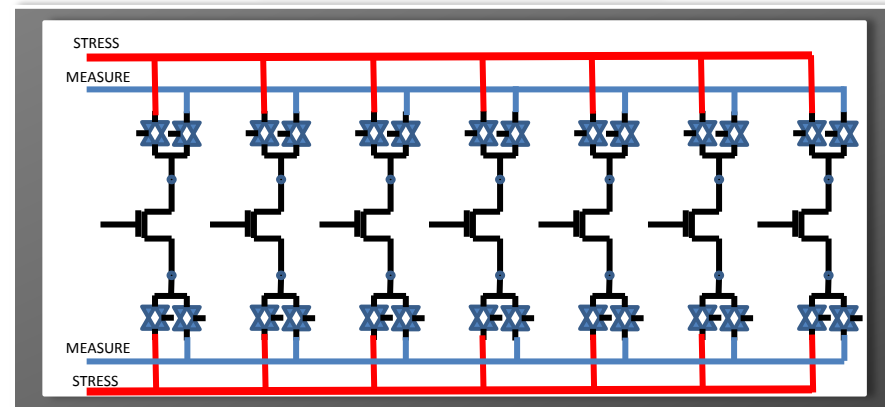
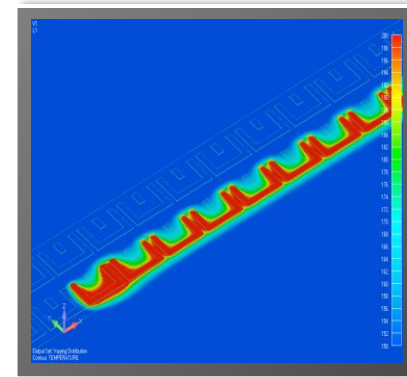
- Peltier device and embedded polysilicon heaters elevate/reduce DUT thermal stress from  $-30^{\circ}\text{C}$  to over  $300^{\circ}\text{C}$
- 4 terminals available to apply electrical stress to each DUT

## Multiple Measurements In Parallel

- High throughput
- Parallel test of 32 – 1024 devices
- Test time reduced from months to hours

## Parallel Test Systems

- Up to 8 benchtop instruments may be controlled from a single PC



Computer GUI  
» Test Type  
» Result Collection  
» Result Processing

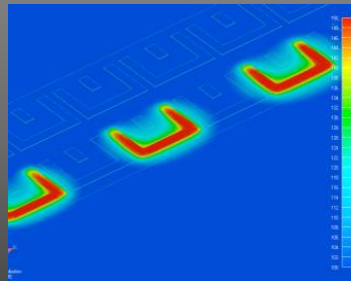
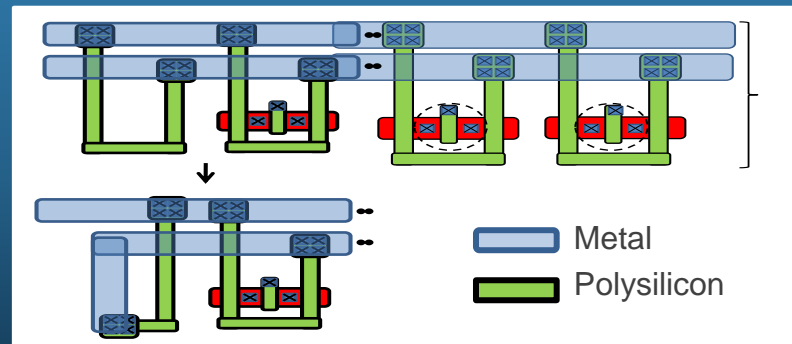


USB 2.0



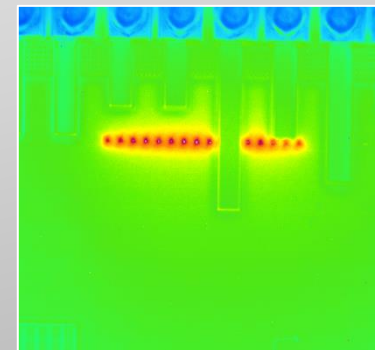
# Local Heating Structures

- Polysilicon tracks are used to create a border around each DUT.



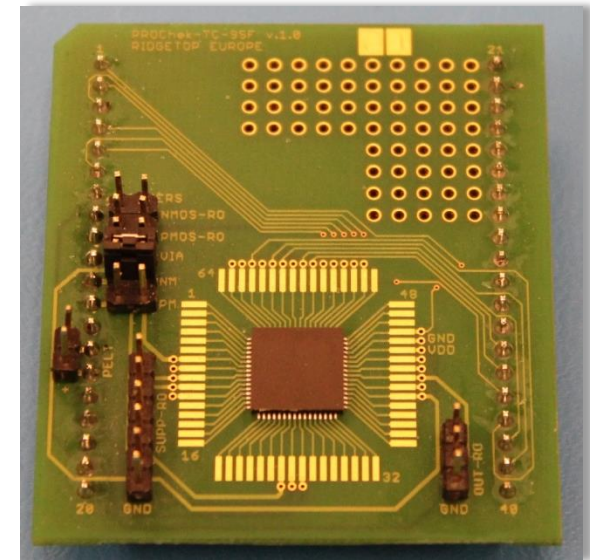
- Localized DUT heaters reach maximum temperature in milliseconds. Non-stressed structures do not undergo any damage.
- Current is forced through these resistive elements to heat the area around the DUTs to over 300 °C.

- Infrared camera data from embedded heating test from IBM 8HP test coupon
- Increasing temperatures will reduce EM, SM and BTI test time and cost

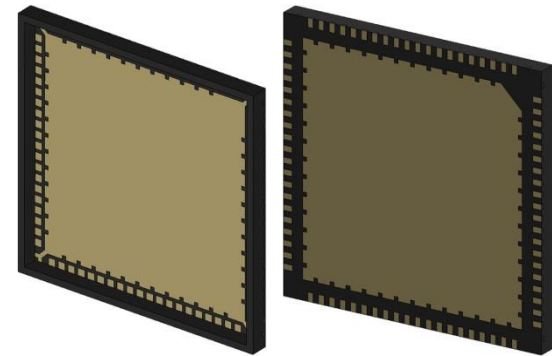


# ProChek Test Coupon

- The Test Coupon contains the DUTs, heaters, temperature sensors, switches and control structures (the on-chip switching matrix) necessary for performing reliability test with the ProChek Benchtop Tester.
- Coupons are packaged in open cavity Plastic or Ceramic packages.
- Packages must have an exposed thermally conductive bulk (usually copper) to ensure good heat conduction.



Packaged ProChek Test Coupon assembled on ProChek Test Card

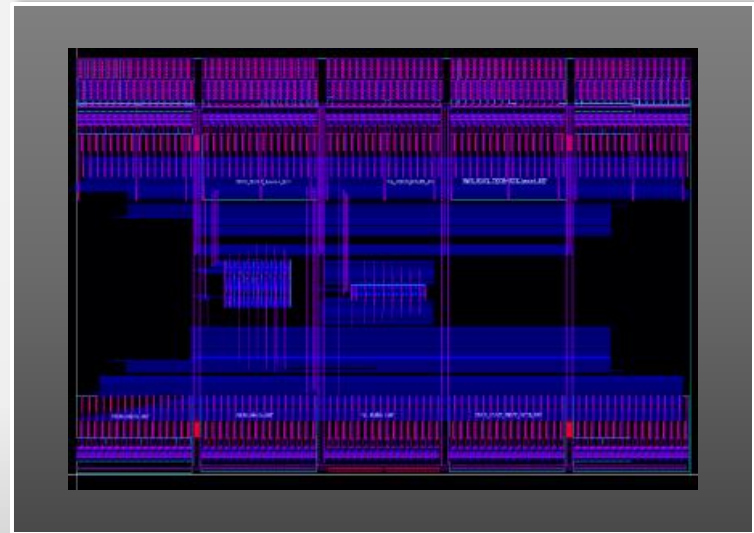


Top and bottom view of package

# Types of ProChek Test Coupons

## Integrated Test Coupon

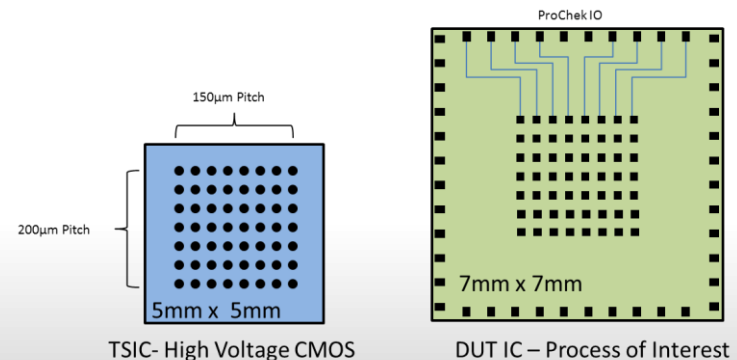
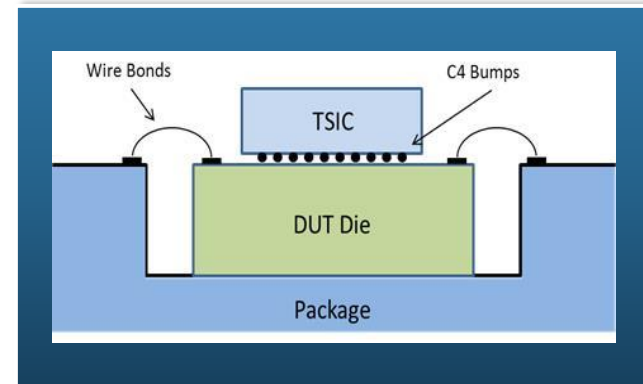
- DUT test structures, control, selection logic, switches, and heaters on a single die.
- Requires both:
  - “Mature”, well defined process, for which there is a stable and well-qualified PDK
  - Process featuring more robust transistors than the DUT test structures



# Types of ProChek Test Coupons

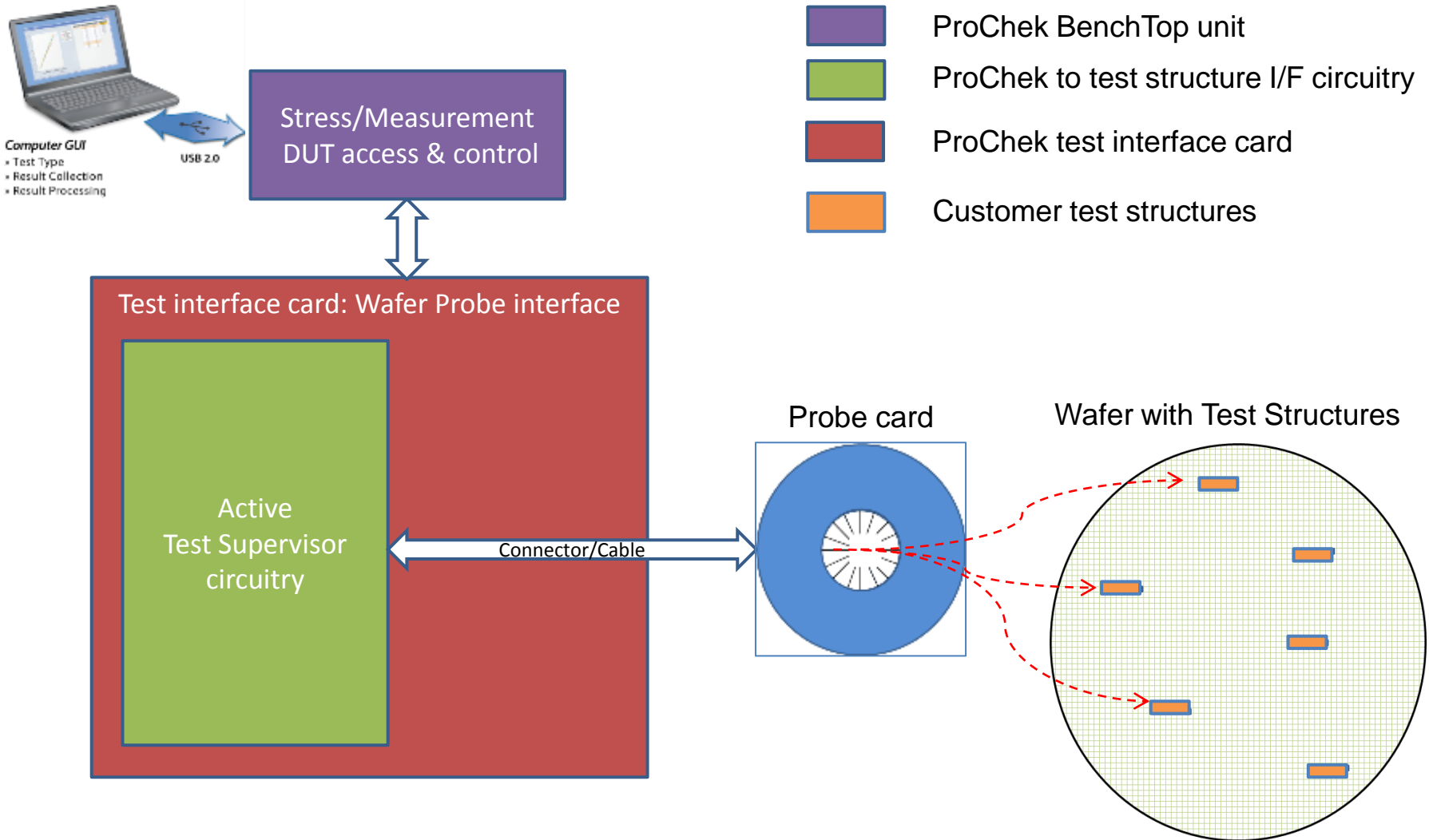
## Test Supervisor IC + DUT IC

- A combined Test Coupon solution consists of a Test Supervisor IC (TSIC) and one or more DUT ICs.
- TSIC:
  - Contains Control and Switching matrix
  - separate die in a mature, higher voltage process.
- DUT IC:
  - DUT structures and heaters
  - separate die using the process of interest.
- The two dies are combined in a single package.





# Customized Wafer Probe Interface



# ProChek Software Interface

ProChek Test Configurator - Untitled\*

File Test System View Help

Test Flow

Phase 1

100x

Phase 2

60x

STOP

Global settings

Supplies Technology TC

Vtc: 5.000 [V]

Vlogic: 0.000 [V]

DUT Selection Temperature Log

DUT block NMOS

Sequential Test Concurrent Test

1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31

2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32

Select All Deselect All

Test Settings

Phase 1 Phase 2

Timing & Heat Control Stress Supplies

Loop & Measurement Settings

# Tests: 100 Ref. Meas. Loop Meas.

Stress Phase Control

	Time [h:m:s]	E	T
S1	1 1 0.0	Yes	Yes
S2	0 0 0.0	Yes	No
M		No	No

Heating / Cooling Settings

	DC [V]	Heat [%]	Cool [%]
S1	4.000	100.0	0.0
S2			
M			

Meas Supplies Instruments Annealing Aux

DC Settings

	Mode	V [V]	I [mA]		
Vg	FV	1.200	C +/- 0.04	No	No
Vd	FV	1.200	C 0.000	No	No
Vs	FV	0.000	C -10	No	No
Vb	FV	0.000	C +/- 0.04	No	No

Sweep Settings

	Start	Stop	Step	[ms]
Swp1				
Swp2				

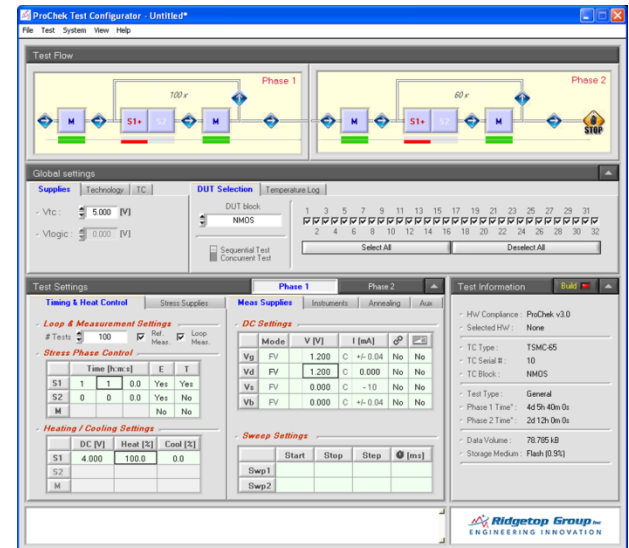
Test Information Build

- HW Compliance: ProChek v3.0
- Selected HW: None
- TC Type: TSMC-65
- TC Serial #: 10
- TC Block: NMOS
- Test Type: General
- Phase 1 Time\*: 4d 5h 40m 0s
- Phase 2 Time\*: 2d 12h 0m 0s
- Data Volume: 78.785 kB
- Storage Medium: Flash (0.9%)

Ridgetop Group Inc. ENGINEERING INNOVATION

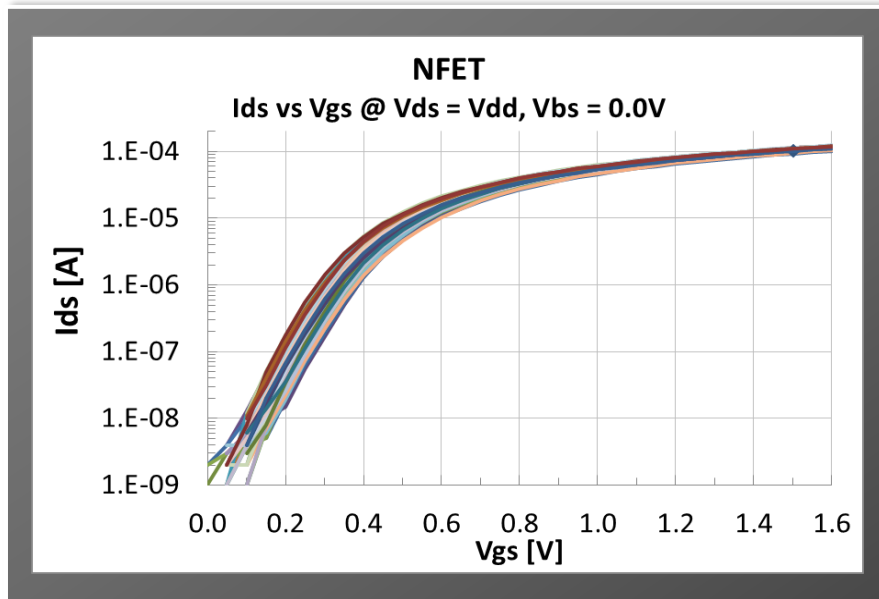
# ProChek Benefits

- Accelerated characterization of new and existing processes
- Ample and accurate process quality information
- Low cost of ownership
- Small, portable, and easy to use

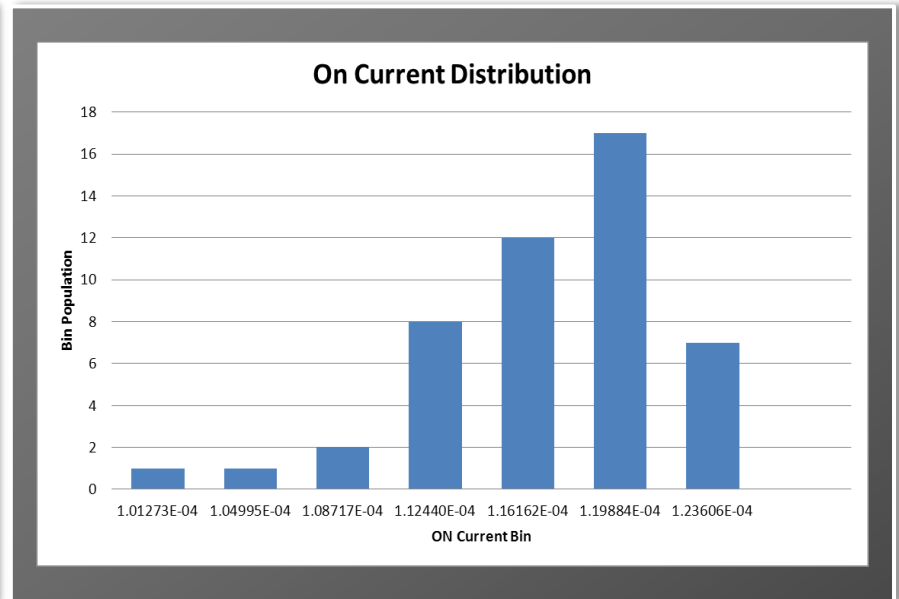


# Bottom Line: ProChek Value

- The ProChek approach allows for a statistical analysis of data relevant to quality monitoring. By increasing the volume of data recorded, a robust analysis can be performed.



$I_{ds}$   $V_{ds}$  curves for 48 NFET DUTs



Distribution of On Current in 48 NFET DUTs

- Slides and recording of the webinar will be available shortly via an e-mail from Ridgetop
- E-mail follow-up questions & comments to:
  - Dr. Jim Lloyd: [jrlloyd@vinfiz.net](mailto:jrlloyd@vinfiz.net)
  - Andrew Levy: [andrew.levy@ridgetopgroup.com](mailto:andrew.levy@ridgetopgroup.com)
- Please fill out our brief feedback survey at <https://www.surveymonkey.com/s/FHM62W9>

Thanks for your time and interest!



# Thank you!

Ridgetop Group, Inc.



3580 West Ina Road  
Tucson, AZ 85741

