IC Process Characterization with ProChek™, a Compact Benchtop System

By

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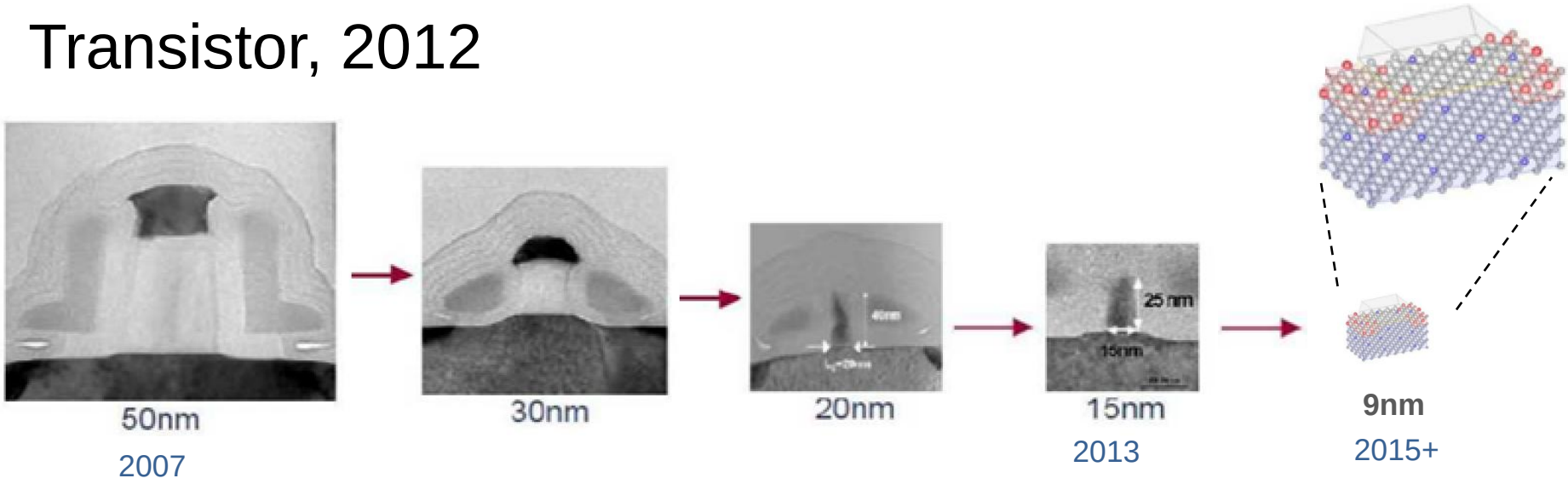
History of Integrated Circuits

First transistor, 1947

Size: 10 cm
Speed: Slow
Circuit Density: 0.0001 devices per 1 mm^2

History of Integrated Circuits

Transistor, 2012

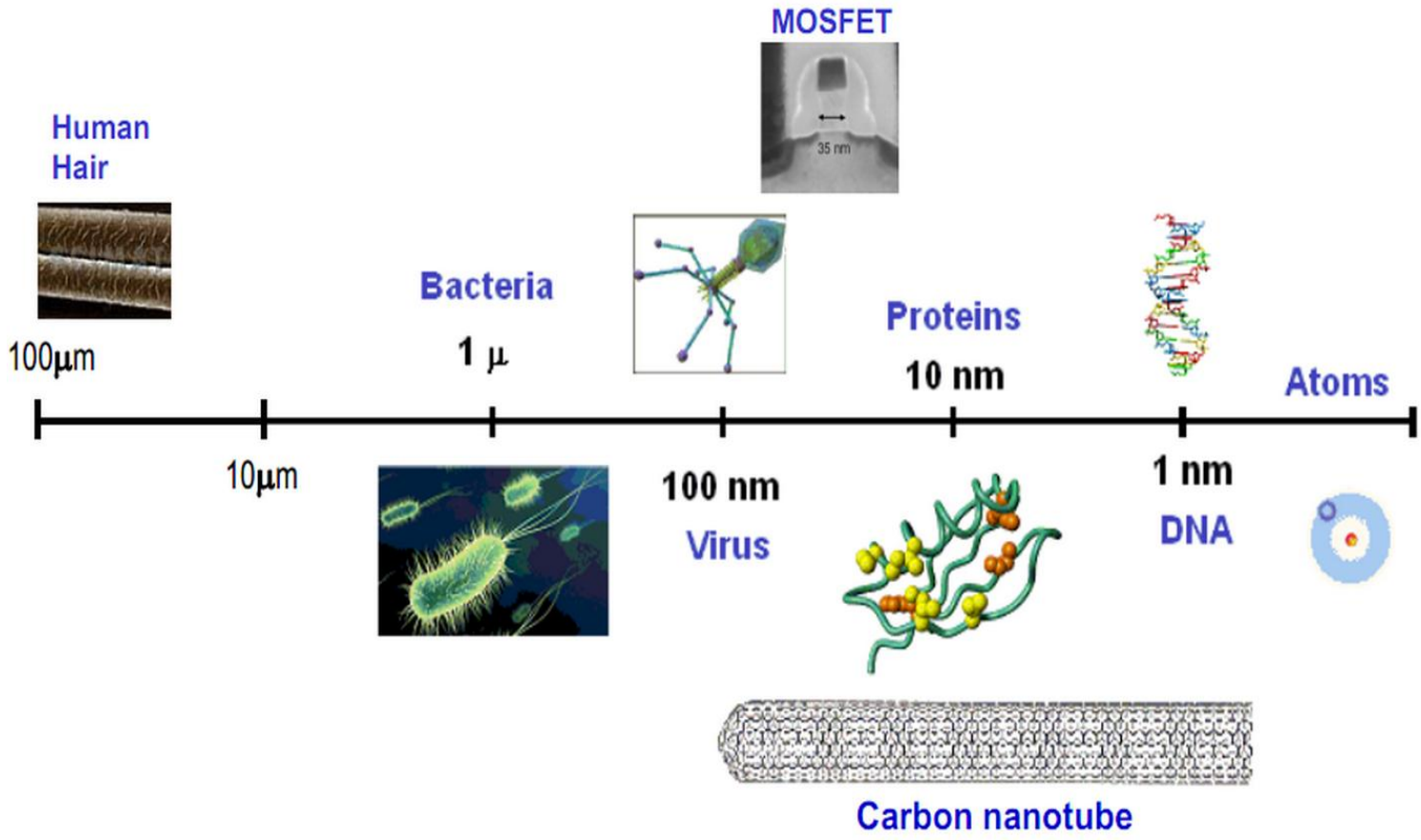


Size: 14 nm
Speed: >500 GHz
Circuit Density: 50,000,000 devices per 1 mm^2

500,000,000,000X improvement in circuit density in 65 years!

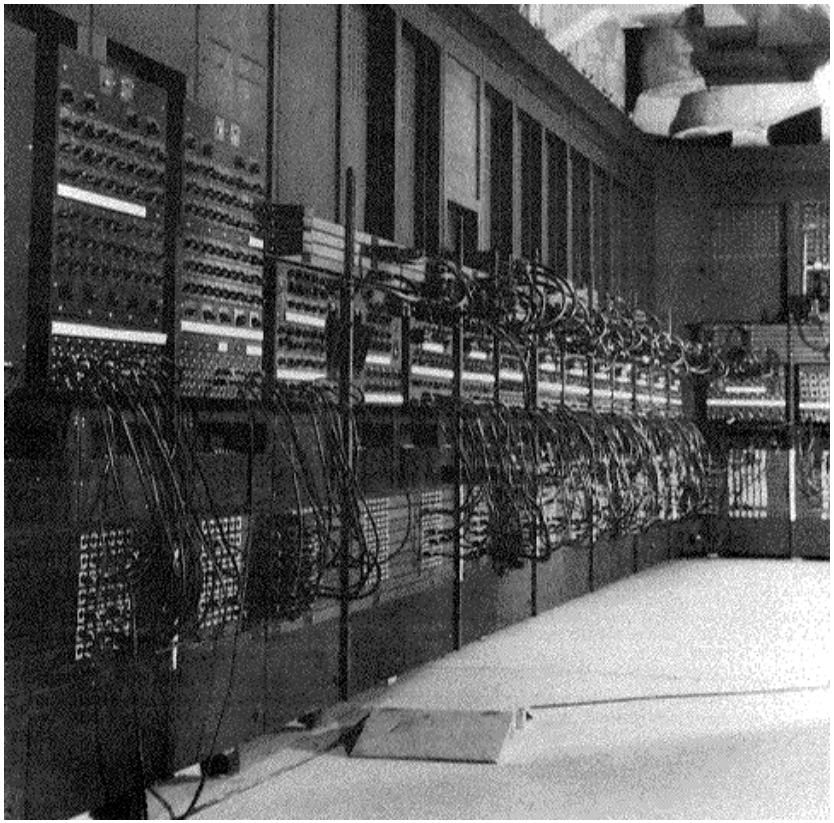
History of Integrated Circuits

Size comparison, 35 nm MOSFET shown



History of Integrated Circuits

First “super computer,” 1947
(ENIAC, “the Giant Brain”)

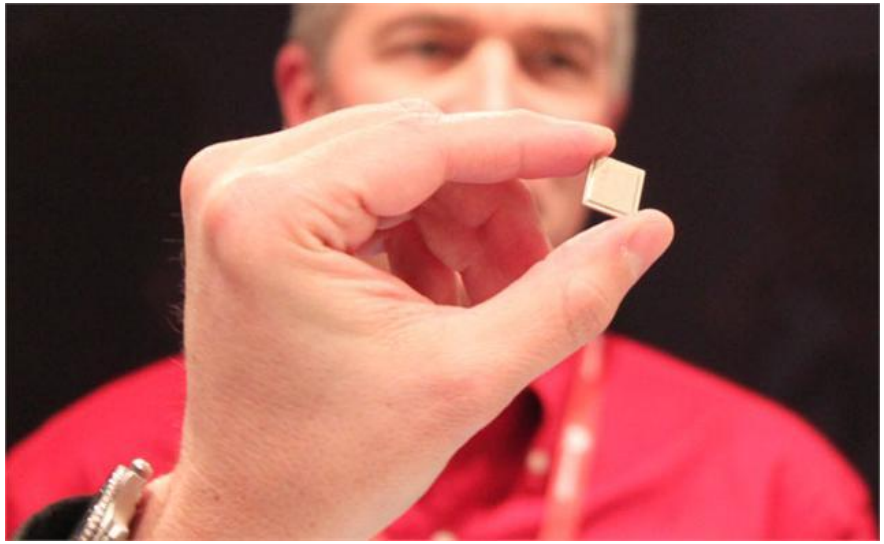


Size: 1800 square feet
Performance: 5,000 FLOPS
Power: 150 kW
Reliability: >10 years

“Where a calculator on the ENIAC is equipped with 18,000 vacuum tubes and weighs 30 tons, computers of the future may have only 1,000 vacuum tubes and perhaps weigh 1½ tons.” – *Popular Mechanics, March 1949.*

History of Integrated Circuits

Microprocessor 2012



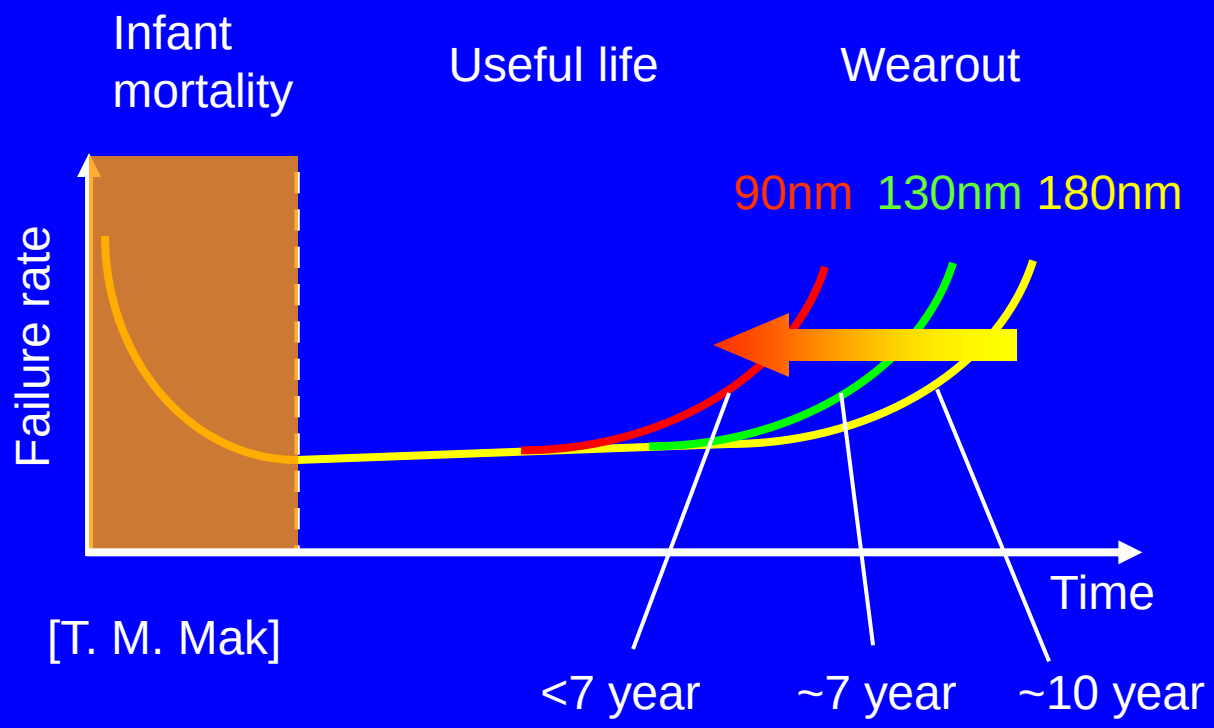
Size: 200 mm^2
Performance: 1,000,000,000,000 FLOPS
Power: 100 W
Reliability: 10 years?

300,000,000,000X improvement in wattage/FLOP in 65 years!

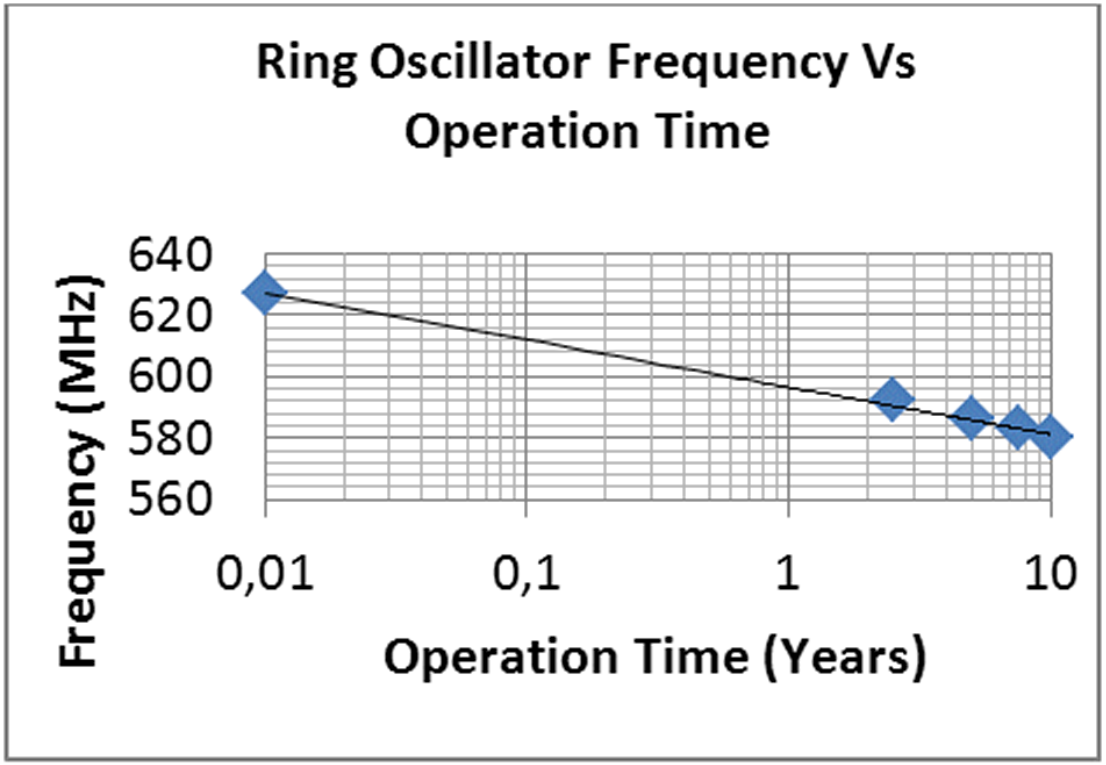
How about reliability?

Trends in IC Reliability

IC lifetime is becoming a serious concern



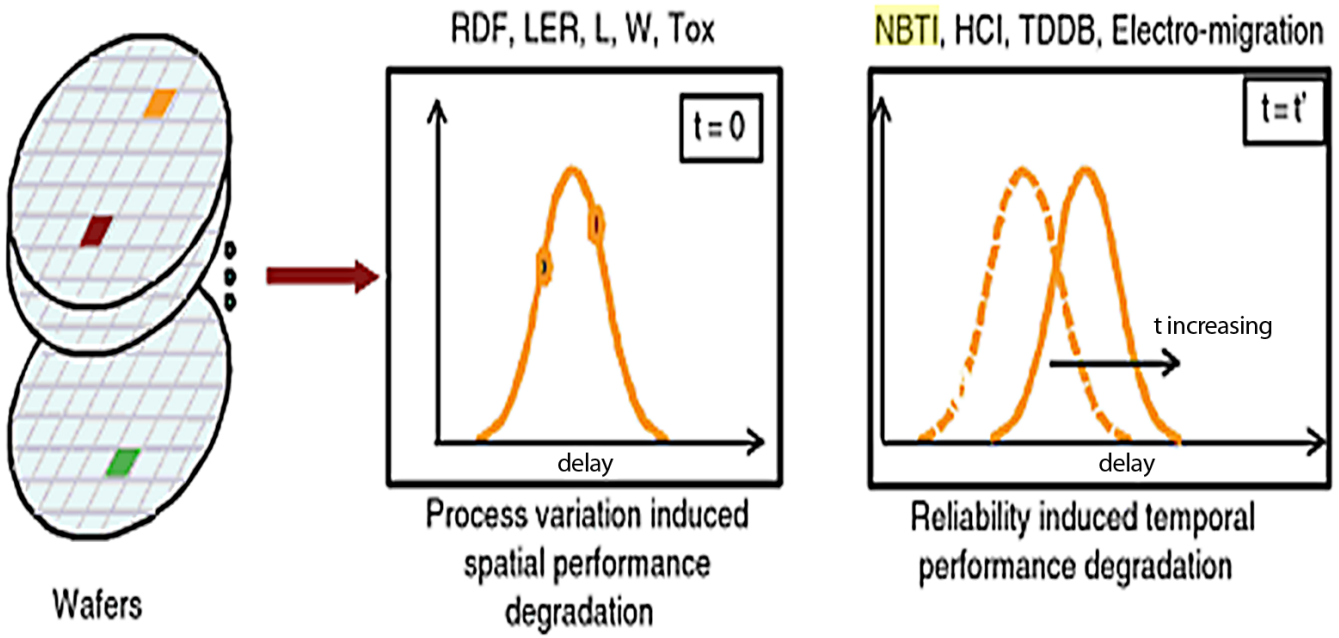
Trends in IC Reliability



28 nm CMOS ring oscillator frequency degrades 5.5% within a year in normal operation conditions

Source: Synopsys

Trends in IC Reliability: Reliability and Process Mismatch



Time-zero parameter spread due to process mismatch shifts during the operational life due to degradation. Both process mismatch and degradation effects are worse in the smallest-geometry processes.

Source: “Low-Power Variation-Tolerant Design in Nanometer Silicon” By Swarup Bhunia

Cost of Reliability Problems

B-2 bomber crash in Guam Feb 2008.

- $1.4B loss

Moisture in the transducers during calibration distorted the information in the air data system.

This caused the flight control computers to calculate inaccurate airspeed and negative angle of attack upon takeoff.

http://telstarlogistics.typepad.com/telstarlogistics/2008/08/photos-and-vide.html

Cost of Reliability Problems

SANTA CLARA, Calif., Jan. 31, 2011 – As part of ongoing quality assurance, Intel Corporation has discovered a design issue in a recently released support chip, the Intel® 6 Series, code-named Cougar Point, and has implemented a silicon fix. In some cases, the Serial-ATA (SATA) ports within the chipsets may degrade over time, potentially impacting the performance or functionality of SATA-linked devices such as hard disk drives and DVD-drives. The chipset is utilized in PCs with Intel's latest Second Generation Intel Core processors, code-named Sandy Bridge. … Intel expects this issue to reduce revenue by approximately **$300 million** as the company discontinues production of the current version of the chipset and begins manufacturing the new version. Full-year revenue is not expected to be materially affected by the issue. Total cost to repair and replace affected materials and systems in the market is estimated to be **$700 million**.

Source: Intel Newsroom

Degradation Effects, Overview

Failure Mode	Physics	System Effect
NBTI (PMOS), PBTI (NMOS)	▪ Negative V_T shift for PMOS, positive for NMOS ▪ Lower leakage and I_{ON}, slower speed	▪ Timing faults in processors other digital circuits ▪ Resettable – but increasing severity over time

TDDB	▪ Soft breakdown:
	  ▪ Slower speed
	  ▪ Weakened gate oxide
	  ▪ Increased leakage current
		▪ Increased ESD vulnerability
		▪ Non-resettable timing faults

	▪ Hard breakdown	▪ Catastrophic short
Hot Carrier (NMOS)	▪ Positive V_T shift ▪ Change in sub-threshold swing (transistor won't turn OFF)	▪ Increased Off-state power ▪ Increased current draw ▪ Decreased data retention time in DRAM
Metal Migration	▪ Higher resistance in Via connections ▪ Open circuits	▪ Catastrophic open

Via/metallization Failure Mechanisms: Electromigration and Stress Migration

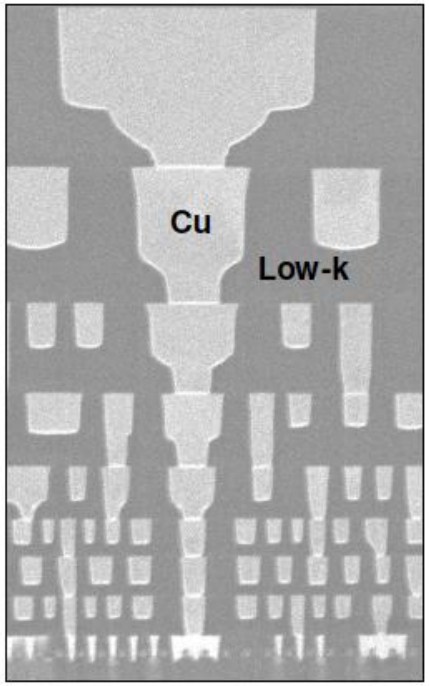
45 nm Interconnects

Loose pitch + thick metal on upper layers

- High speed global wires
- Low resistance power grid

Tight pitch on lower layers

- Maximum density for local interconnects



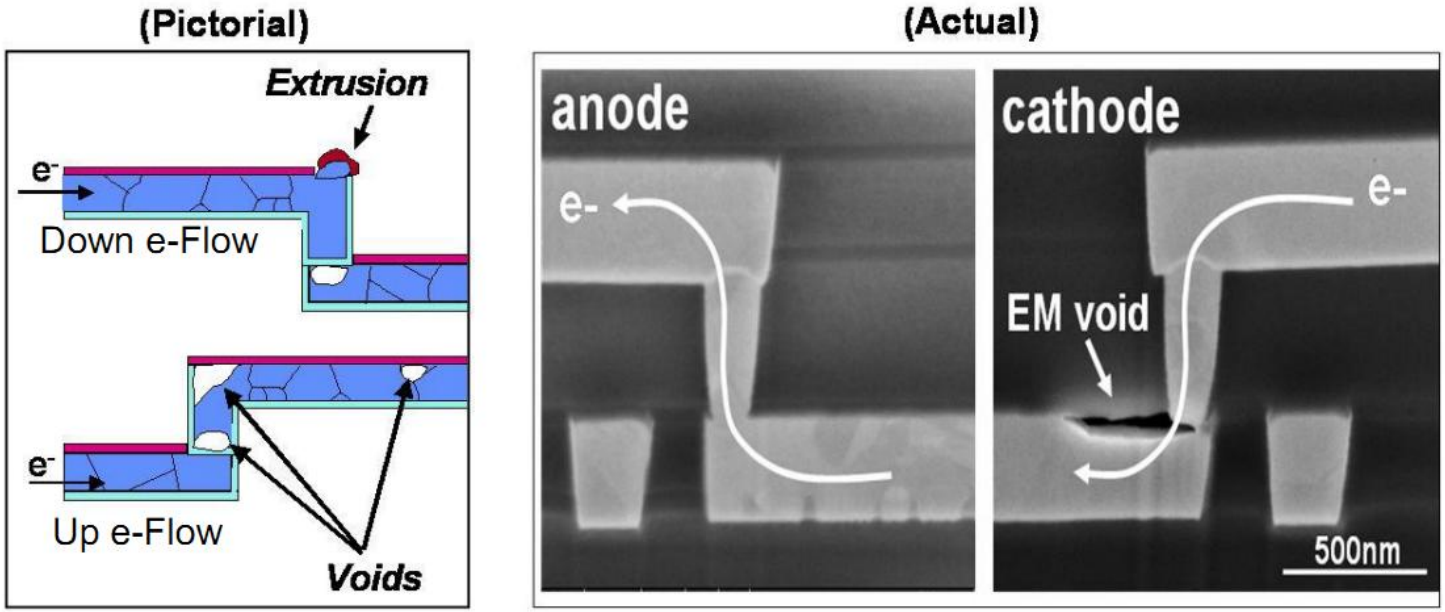
	Pitch (nm)
M8	810
M7	560
M6	360
M5	280
M4	240
M3	160
M2	160
M1	160

Hierarchical interconnect pitches

Modern CMOS processes have several metallization layers (up to a dozen).

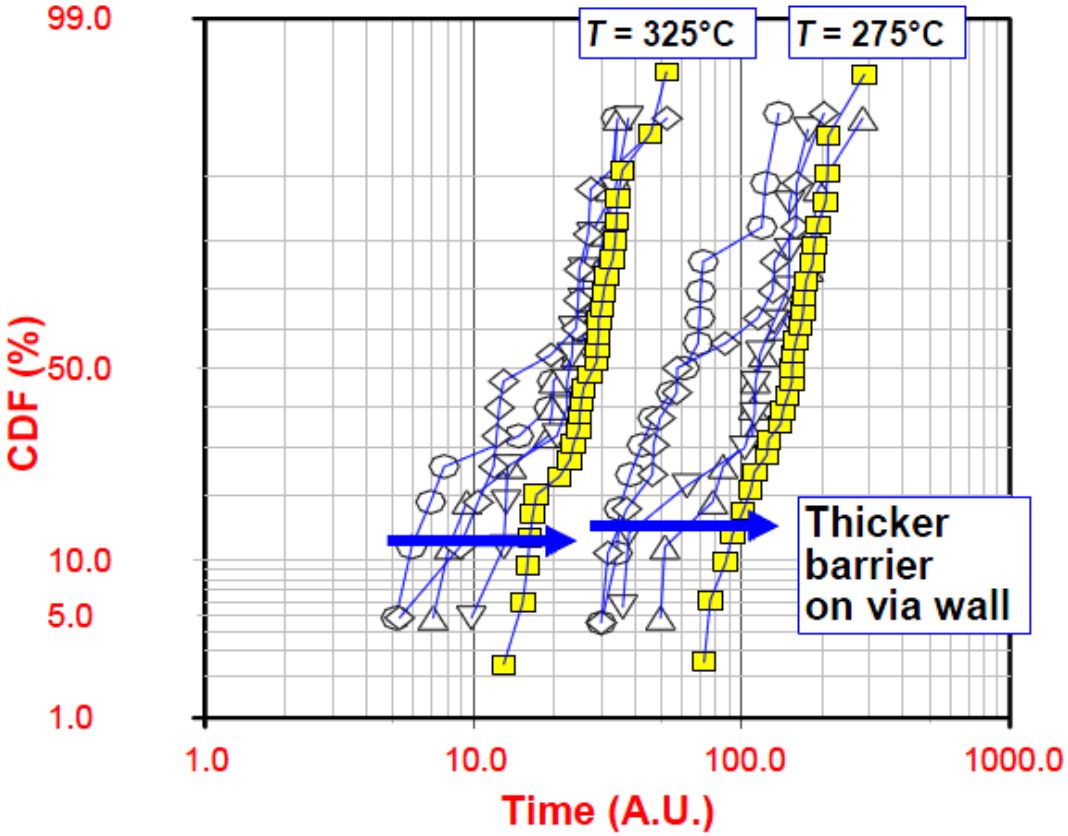
Degradation Mechanisms: Electromigration

Electromigration Associated with Vias



Source: IRPS 2011 Tutorials

Electromigration (Temperature Dependency)

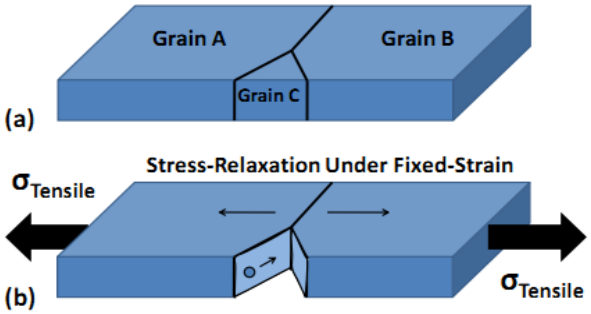


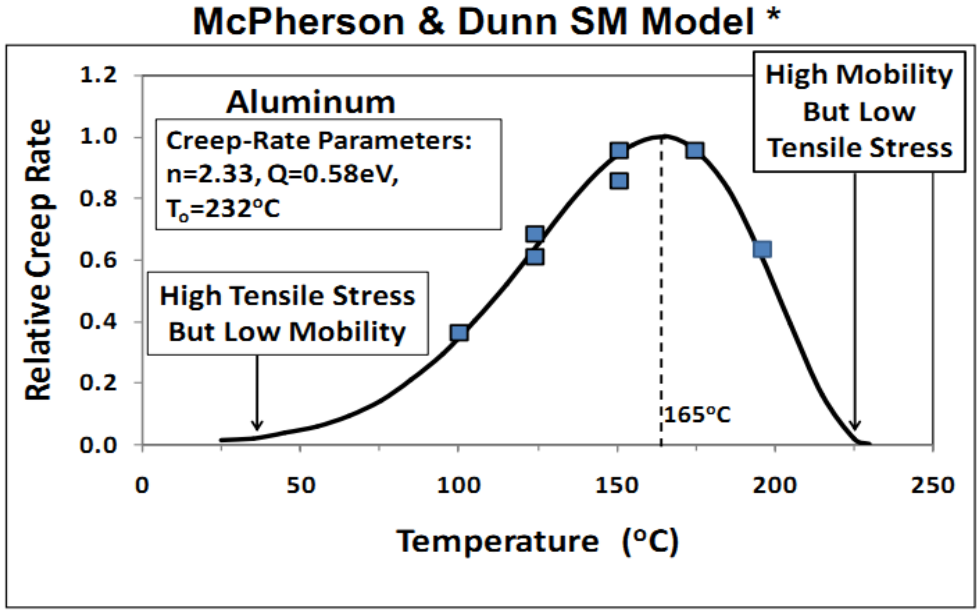
Reported data from fast Wafer Level Reliability (fWLR) tests shows that every 50 C increase in the stress temperature will reduce the electromigration testing time by one order of magnitude.

Source: Ki-Don Lee, et al., "VIA PROCESSING EFFECTS ON ELECTROMIGRATION IN 65 NM TECHNOLOGY", 44th Annual International Reliability Physics Symposium, San Jose, 2006.

Stress Migration (Al Metallization)

Stress-Migration/Voiding-Rate in Al Metallization





$$Creep(Voiding)Rate = B_o\,(T_o - T)^n \exp\left[-\frac{Q}{K_B T}\right]$$

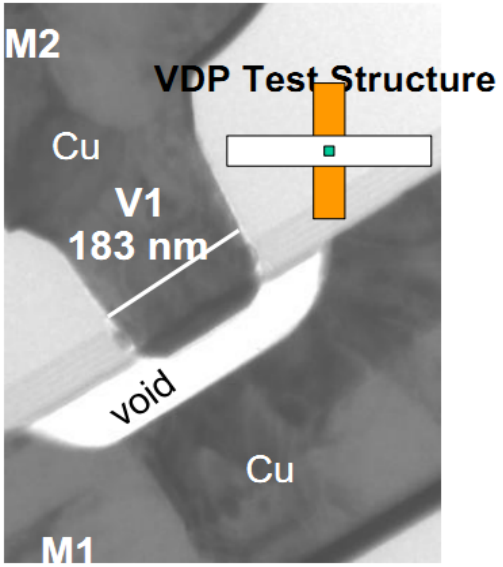
* J. McPherson and C. Dunn, "Model for Stress-Induced Metal Voiding in Al-Metallization", J. Vacuum Sci. & Technology B, 1321 (1987).

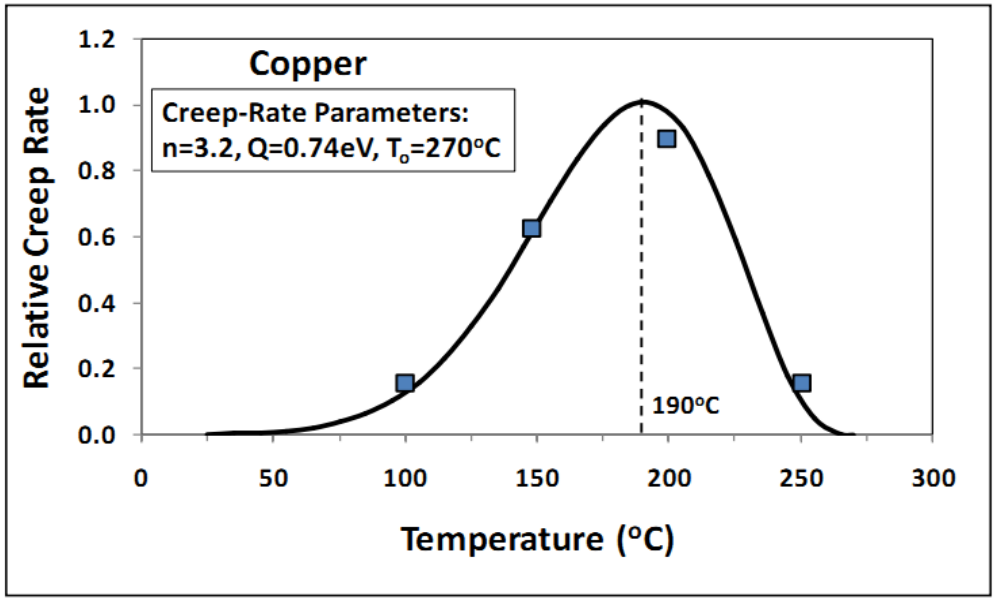
Conclusion: Peak occurs in the SM Rate for Al from 150-175°C.

Source: IRPS 2011 Tutorials

Stress Migration (Cu Metallization)

Stress-Migration/Voiding-Rate in Cu





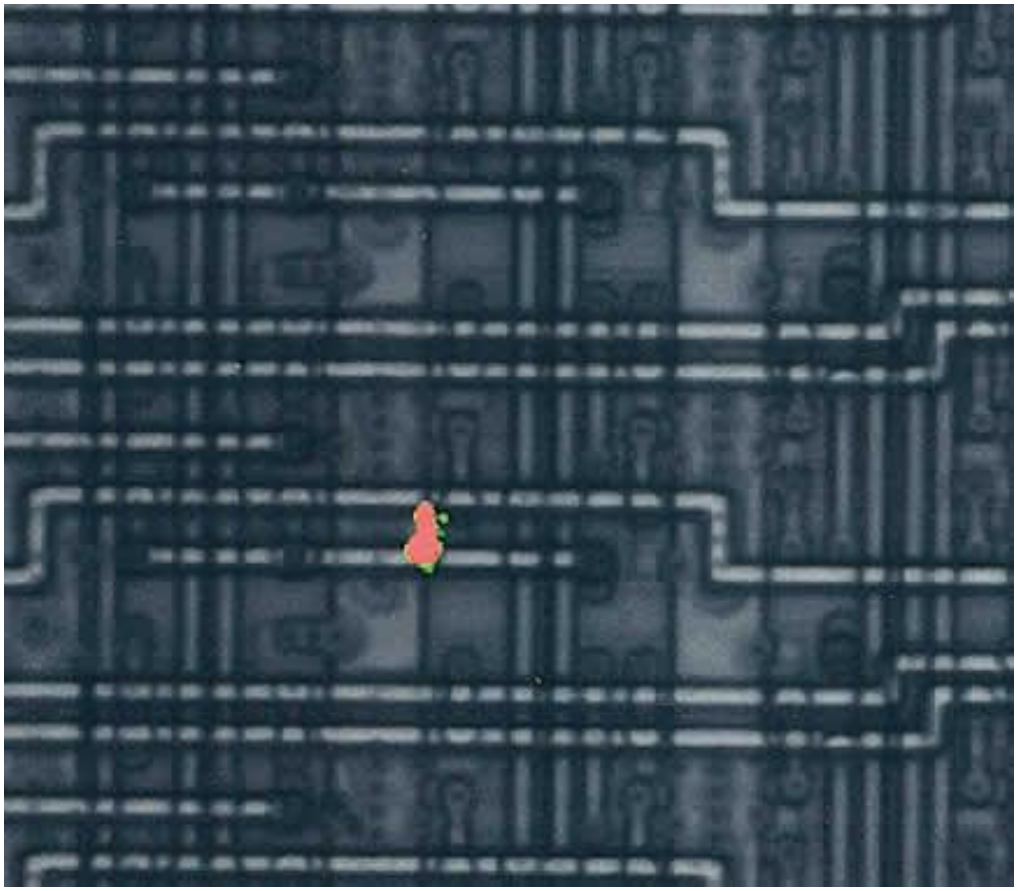
[TI: E. Ogawa and J. McPherson, IEEE-IRPS, 312(2003)

$$Creep(Voiding)Rate = B_o\ (T_o - T)^n\ \exp\left[-\frac{Q}{K_B T}\right]$$

Conclusion: Peak occurs in the SM Rate for Cu from 175-200°C.

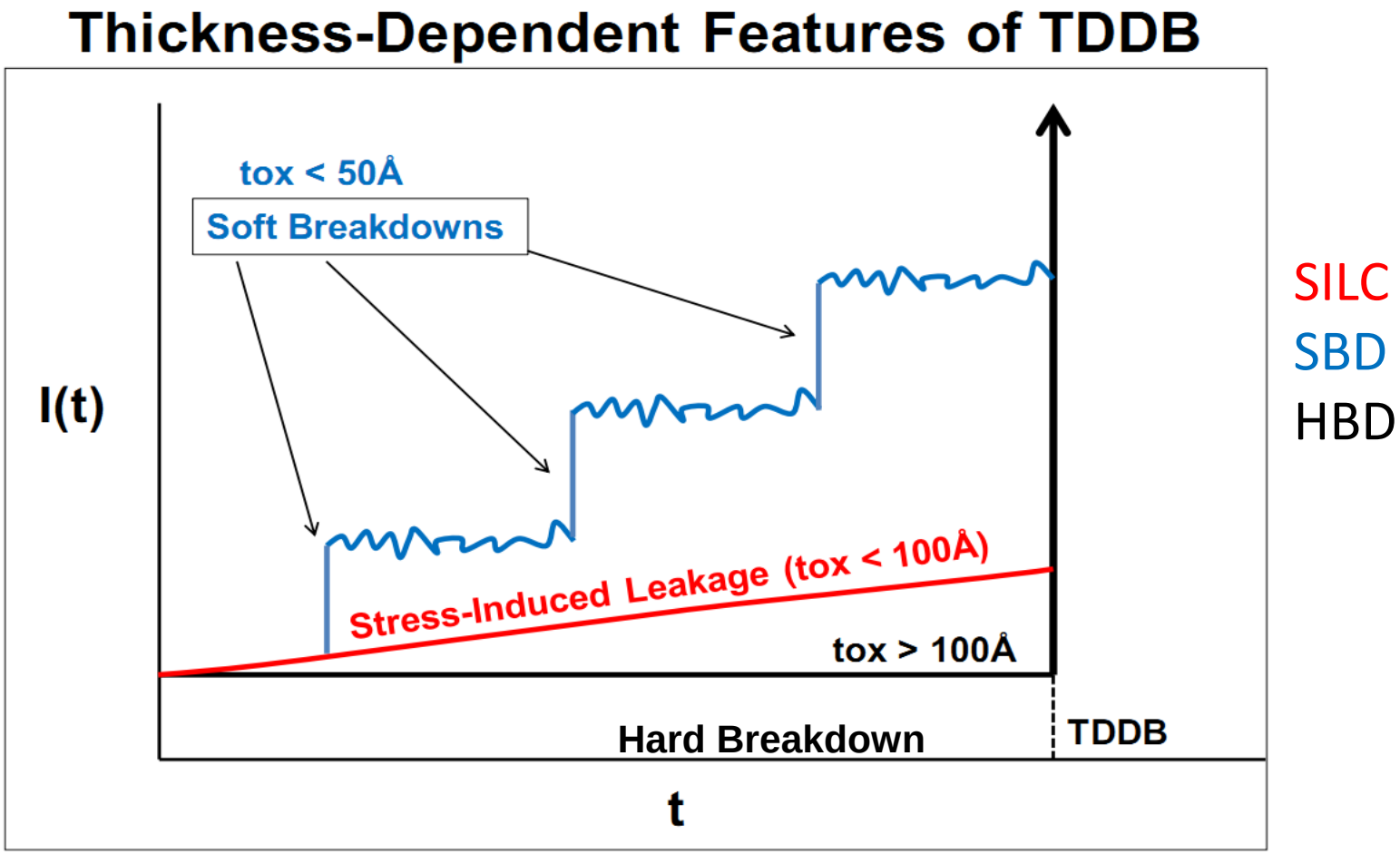
Source: IRPS 2011 Tutorials

Time-Dependent Dielectric Breakdown (TDDB)



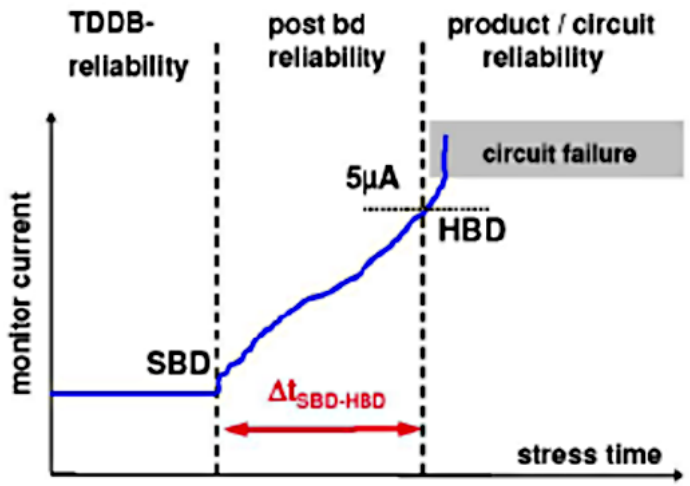
Short caused by TDDB is seen in this thermal camera image.

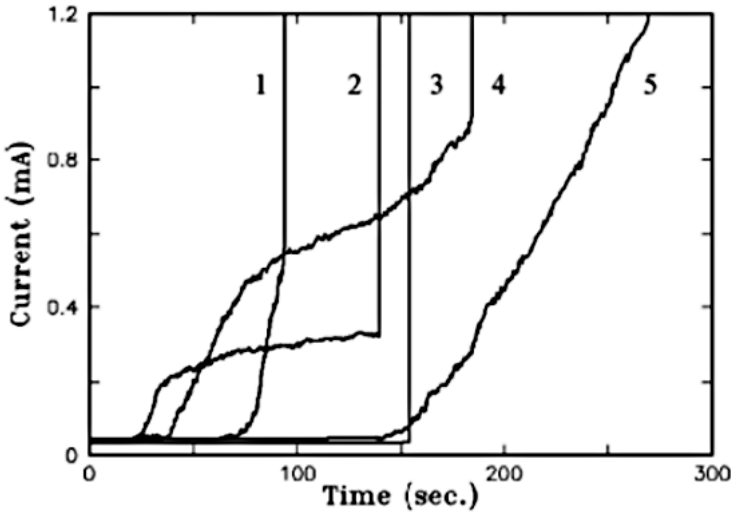
TDDB (Types of Breakdown)

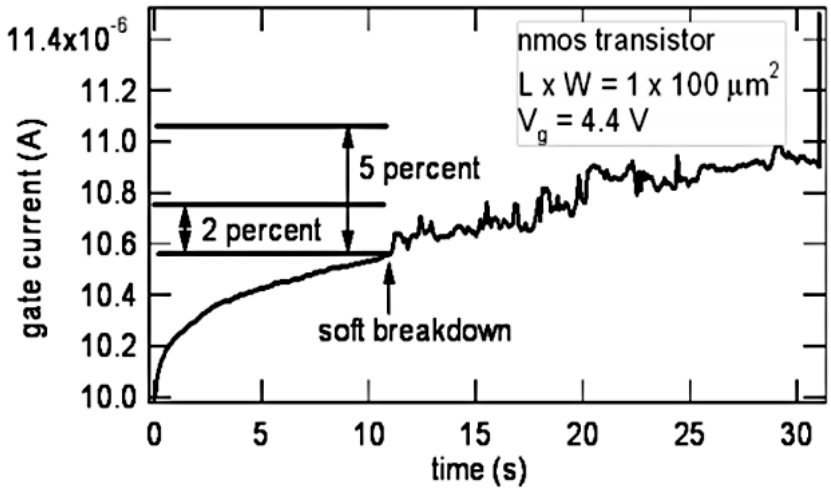


Source: IRPS 2011 Tutorials

TDDB (Types of Breakdown)



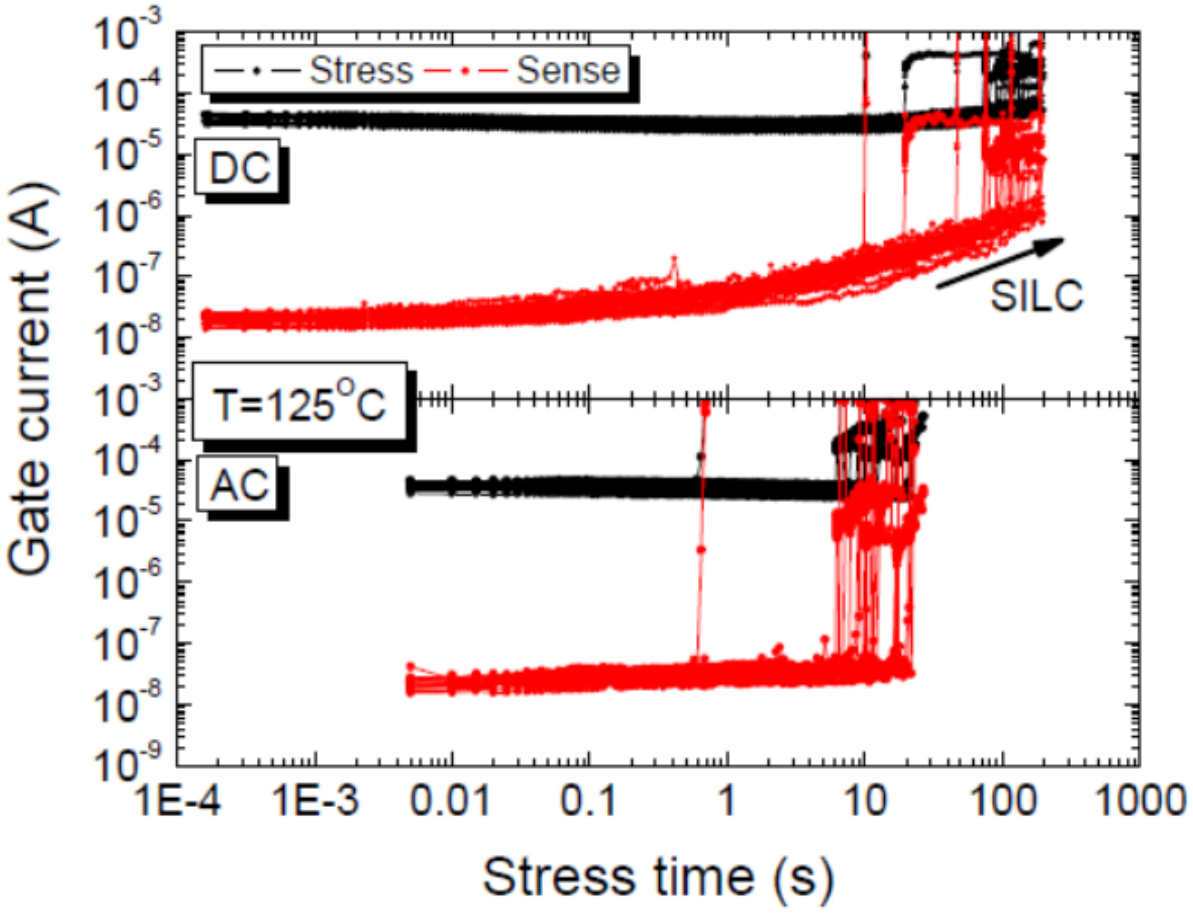




Criteria between TDDB types are not well-defined.

Source: IRPS 2011 Tutorials

TDDB (DC stress vs. AC stress)



DC and AC stresses may cause completely different results => Need to characterize both stress modes.

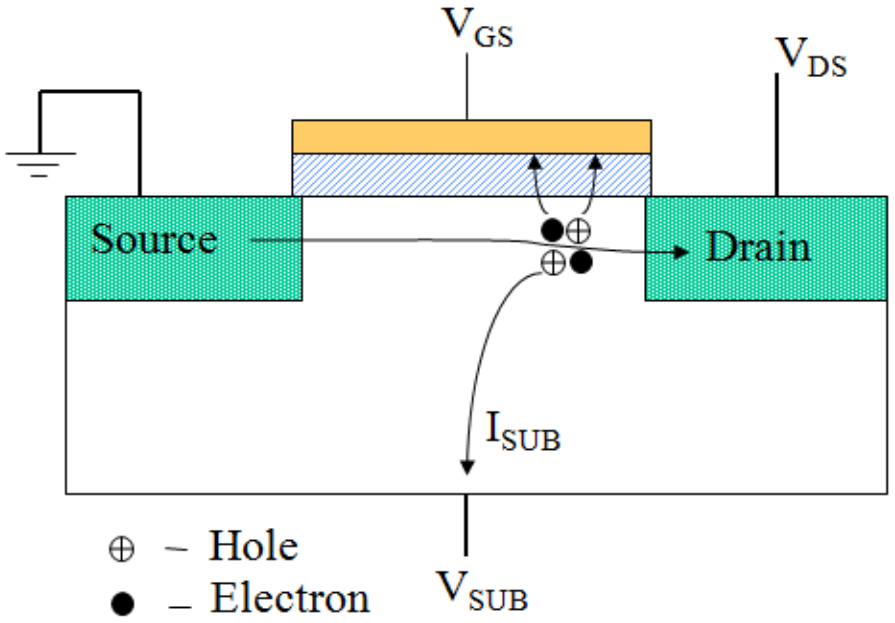
Source: IRPS 2011 Tutorials

Hot Carrier Degradation

Hot Carrier – Physics of Failure

Drain Avalanche Hot-Carrier Injection

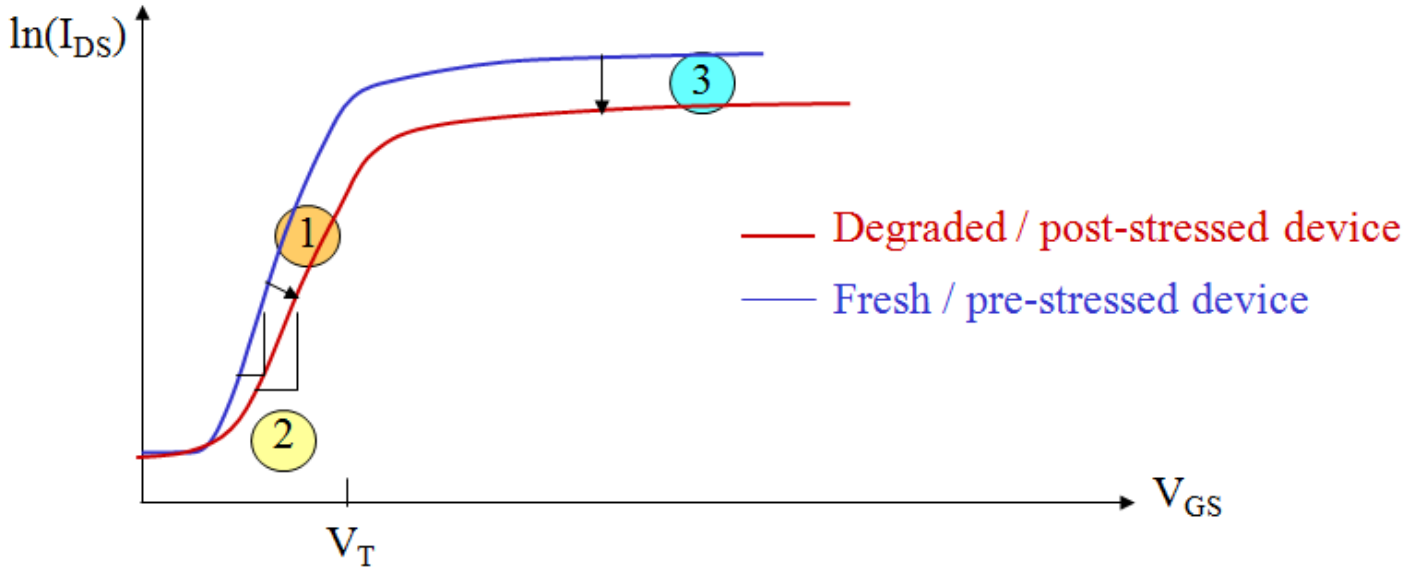
- Impact ionization
  - Energetic electrons excite other e^-'s from VB to CB
  - Holes created at VB
- Holes are attracted toward:
  - Substrate contact
  - Gate oxide (low V_{GS})
- Electrons go toward:
  - Drain contact
  - Gate oxide (mid and high V_{GS})



Ridgetop Group Inc 3580 West Ina Road | Tucson AZ | 85741 | 520-742-3300 | ridgetopgroup.com

Hot Carrier Degradation

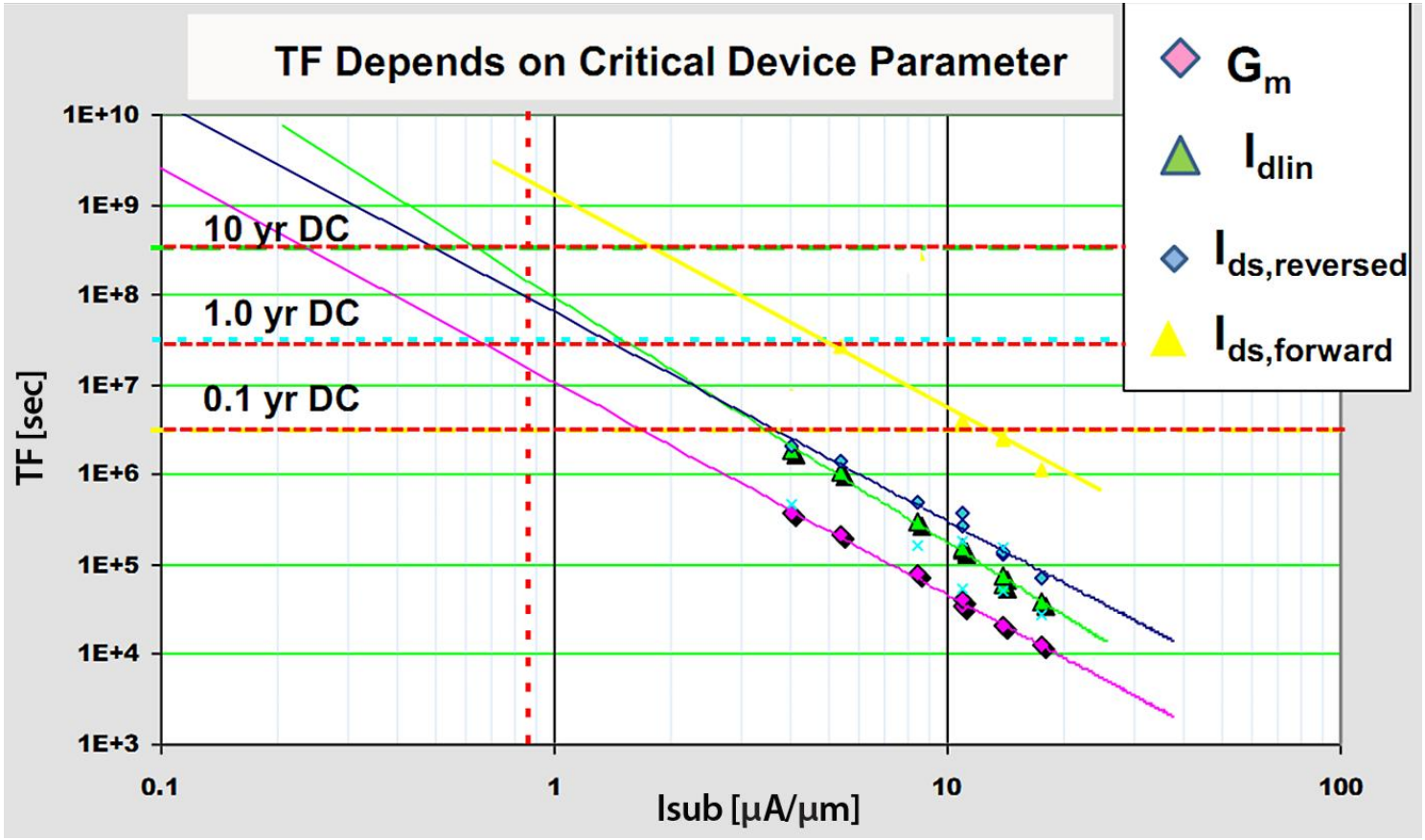
Hot-carrier induced effects



1. Parallel shift of I-V curve due to oxide trapped charge N_{ot} => Increase in V_T
2. Stretch-out of I-V curve due to interface states N_{it} => Decrease in 's'
3. Decrease in transconductance due to mobility degradation => Decrease in I_{Dsat}

Hot Carrier Degradation

HCI Impact on NMOS Device Parameter



Note: Time-To-Failure should be based on the critical device-parameter of interest

Source: IRPS 2011 Tutorials

Hot Carrier Degradation

Fabs do not give enough reliability test data to designers and reliability engineers

Qual Items	DUT	Structures	Sample size	Stress Conditions	Failure Criteria	Specifications	Result
Gate oxide VBD	1.2V Core	Area = 5e2 ~ 2.4e3 um^2	>=3 wafer/lot; 3 lots; 25,560	Voltage ramp 3.3V/s (inversion mode)	Ig leak > 40uA @ 1V	Do <= 5/cm^2 @ VBD <= 1.2V Do <= 1/cm^2 @ 1.2V < VBD < 2.9V	Pass
	2.5V I/O	Area = 4.8e3 ~ 1e6 um^2		Voltage ramp 6.27V/s (accumulation mode)	Ig leak > 15uA @ 1.5V	Do <= 5/cm^2 @ VBD <= 2.5V Do <= 1/cm^2 @ 2.5V < VBD < 5.0V	Pass
	2.5V I/O over drive			Voltage ramp 6.27V/s (accumulation mode)	Ig leak > 15uA @ 1.5V	Do <= 5/cm^2 @ VBD <= 3.3V Do <= 1/cm^2 @ 3.3V < VBD < 7.2V	Pass
Gate oxide TDDB	1.2V Core	Area ~ 1e7 um^2 (W/L=1/0.06)	>= 50/stress/lot; 3 lots	3-5 stress voltage @ 125C & field ~ 8-12MV/cm	1st soft breakdown	TTF @0.1% cum failure rate > 10yr for 0.1cm^2 @ 125C & 1.2V+10%	Pass
	2.5V I/O	Area ~1e6 um^2 (W/L=4/4.8 x 2000)		3-5 stress voltage @ 125C & field ~ 8-12MV/cm	Hard breakdown	TTF @0.1% cum failure rate > 10yr for 0.01cm^2 @ 125C & 2.5V+10%	Pass
	2.5V I/O over drive			3-5 stress voltage @ 125C & field ~ 8-12MV/cm	Hard breakdown	TTF @0.1% cum failure rate > 10yr for 0.01cm^2 @ 125C & 3.3V+10%	Pass
PID	1.2V Core	W/L=5/0.2	>= 4 wafer/lot; 3 lots	Ig @Vg=1.4Vcc inversion	Ig tailing	Ig tailing < 5%	Pass
	2.5V I/O	W/L=2.63/0.38		Ig @Vg=1.8Vcc (2.6Vcc) for NMOS (PMOS)			
HCI	1.2V Core	W/L=1/0.06	24/pattern/lot; 3 lots	1.2V (Vds=Vgs=1.7V, 1.8V, 1.9V, 2.0V) TTF vs 1/Vds	Idsat change > [illegible]%	DC lifetime > 0.2 yr	Pass
	2.5V I/O	W/L=10/0.28	15/pattern/lot; 3 lots	2.5V (Vds=3.3V, 3.5V, 3.7V, Vgs@Isub(max)) TTF vs Isub^m		AC lifetime > 10 yr	Pass
	2.5V I/O over drive	W/L=10/0.5 (N), 10/0.4 (P)		2.5V (Vds=4.1V, 4.3V, 4.5V, Vgs@Isub(max)) TTF vs Isub^m		0.1% cum failure @25C, Vc[illegible]0% (Core P @125C)	Pass
NBTI	1.2V Core	W/L=1/0.06	>= 20/lot; 3 lots	Vg: 6-9 MV/cm @ 125C; Vs=Vd=Vb=grounded	Idsat degrade > 10%	TTF 0.1% cum failure @125C, Vcc+10% >5 yr	Pass
	2.5V I/O	W/L=10/0.28					
	2.5V I/O over drive	W/L=10/0.4					
EM	M1 + contact	W/S=0.09/0.09 (1800 A)	> 20/pattern/lot; 3 lots	Jstess=1-5MA/cm^2 @ 300C	dR >10% Ro	TTF 0.1% cum failure @110C > 100k hr	Pass
	Mx + Vx	W/S=0.10/0.10 (2200 A)					
	My + Vy	W/S=0.20/0.20 (5000 A)		Jstess=1-5MA/cm^2 @ 350C			
	Al-Cu RDL	W/S=3/2 (14.5K A)		Jstess=1-5MA/cm^2 @ 250C			
SM	Vias chain	metal-via overlap from min to 0.7	>130/lot; 3 lots	500 hr bake @175C	dR >10% Ro	No failure allowed	Pass
IMD Low-K TDDB	M1, V1, M2 combs	M1 & M2 W/S=Min/Min V1 W/S=0.10/0.13	>30 /pattern/lot; 3 lots	2.5-4.0 MA/cm @ 125C	I(TBD) = 100 x I(T=0)	TTF 0.1% cum failure @125C & 3.6V > 10 yr	Pass

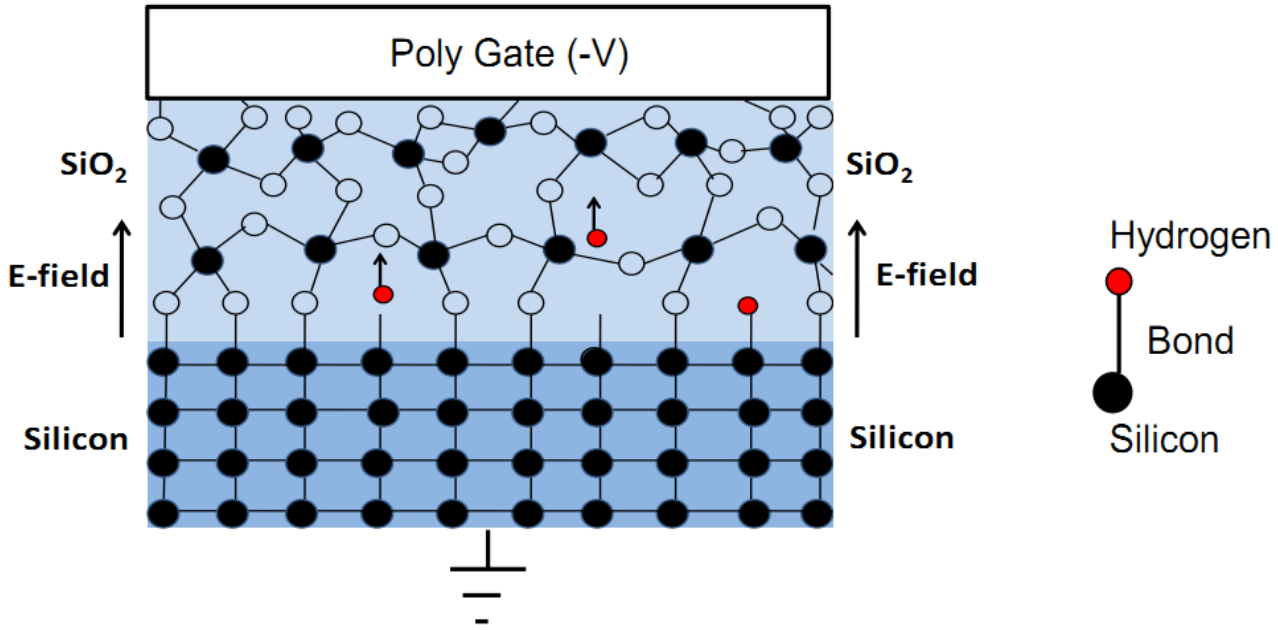
DC lifetime for Hot Carrier >**0.2 yr**, AC lifetime >**10 yr** in a 65 nm CMOS process

http://www.siliconbluetech.com/media/downloads/SBT_65LP_Process_Qual_v0.1.pdf

NBTI and PBTI

Negative-Bias Temperature Instability (NBTI)

P-MOSFET ISSUE

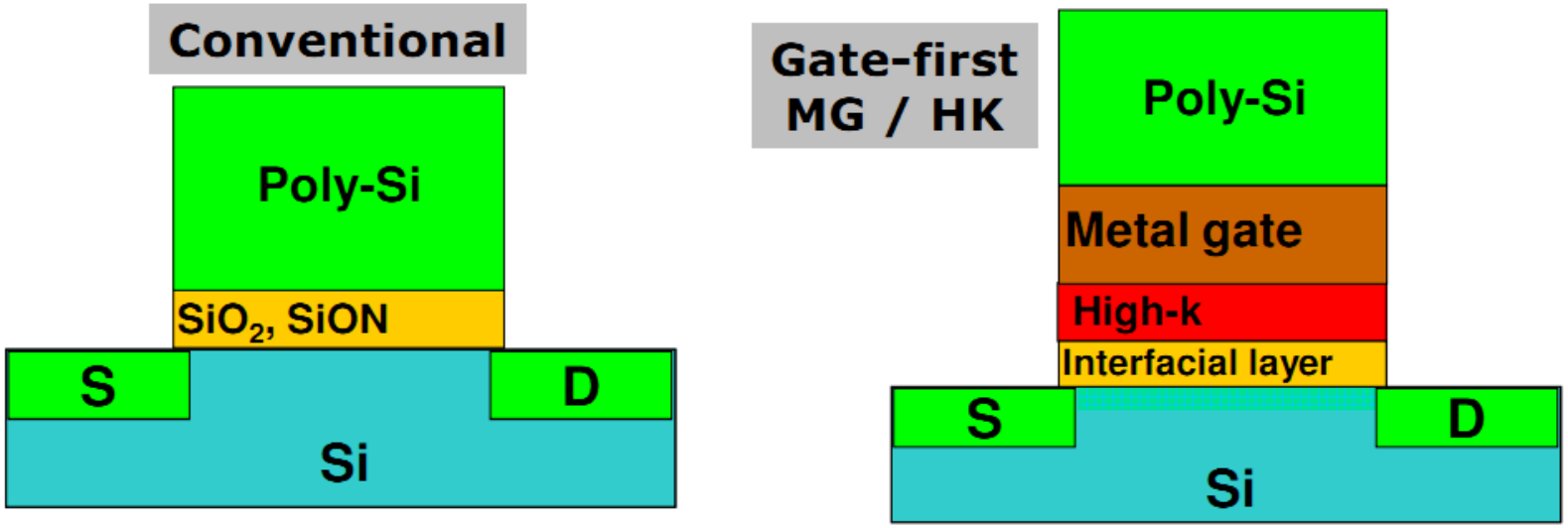


During normal P-MOS operation, interfacial Si-H bonds can become broken. Negative gate voltage serves to produce more holes at the Si surface. Hole absorption by the Si-H bond can serve to free the hydrogen which can then can diffuse away from the Si-O interface resulting in interface-state generation and a V_{th} shift. Si-H bonds are more easily broken at higher temperatures.

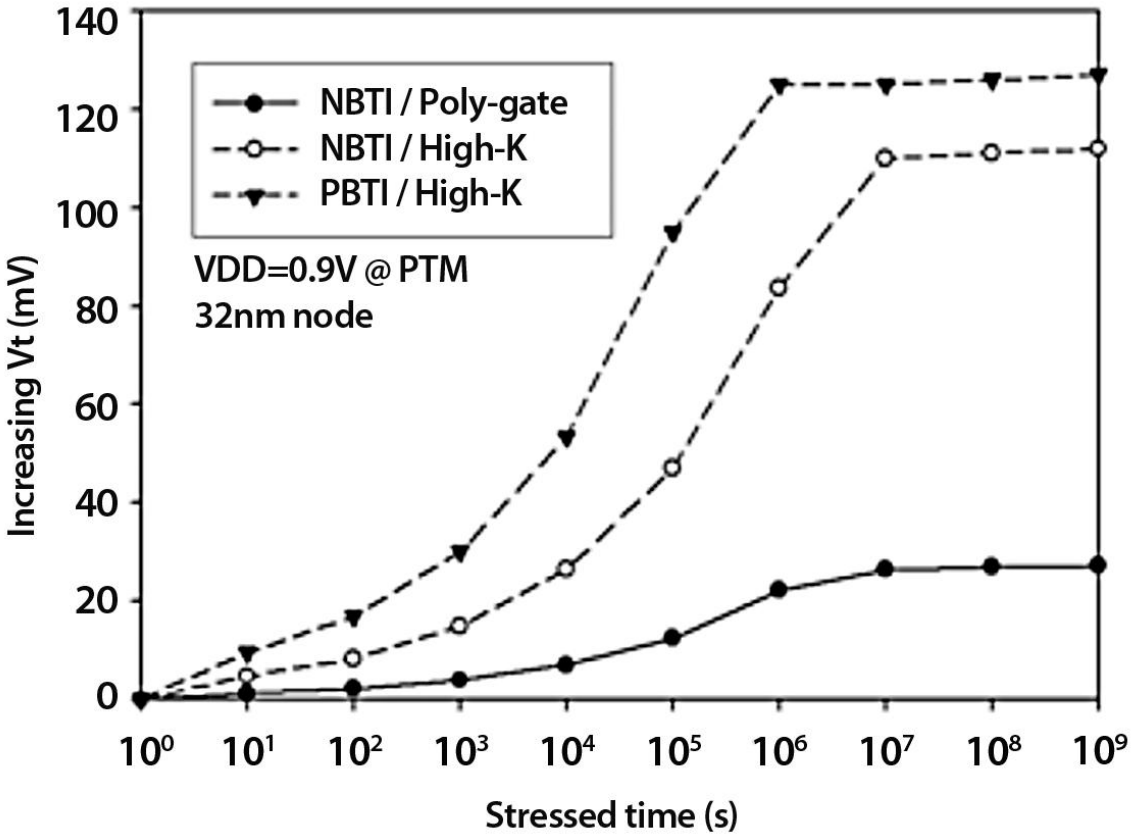
Source: IRPS 2011 Tutorials

NBTI and PBTI (High-K Gate)

PBTI is an issue in the modern “High K + Metal Gate” technologies



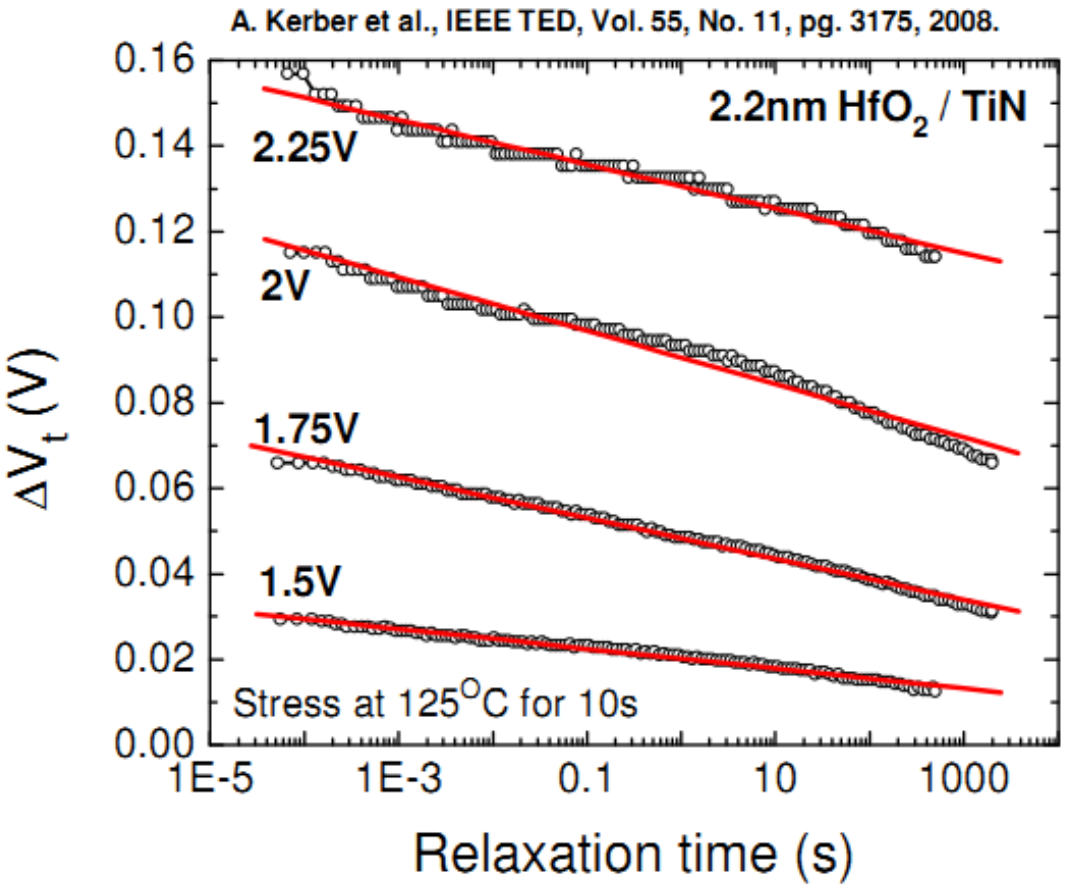
NBTI and PBTI (High-K Gate)



NBTI/PBTI-induced V_T drifts vs. stressed time for 32 nm poly-gate and high-k metal-gate devices.

Source: Shyh-Chyi Yang, et. Al TIMING CONTROL DEGRADATION AND NBTI/PBTI TOLERANT DESIGN FOR WRITE-REPLICA CIRCUIT IN NANOSCALE CMOS SRAM, VLSI-DAT '09.

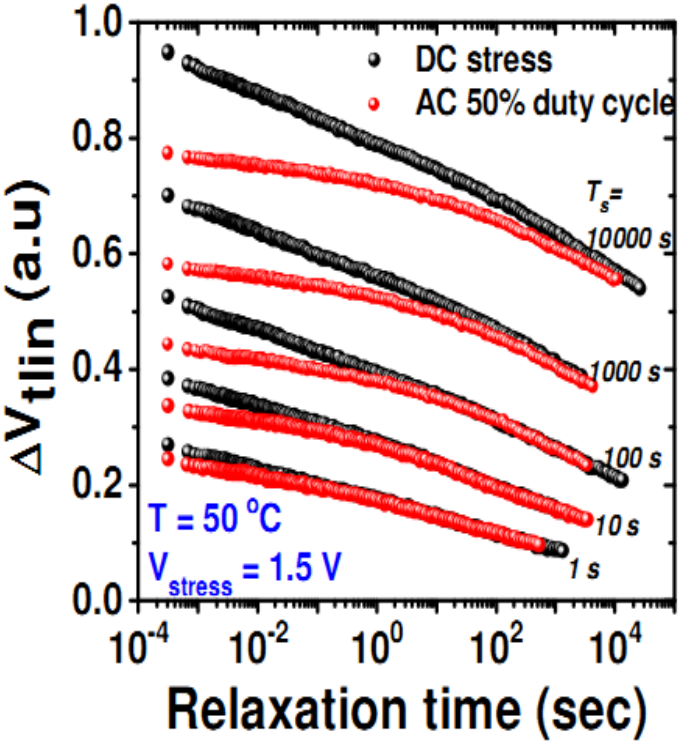
NBTI and PBTI (Relaxation)

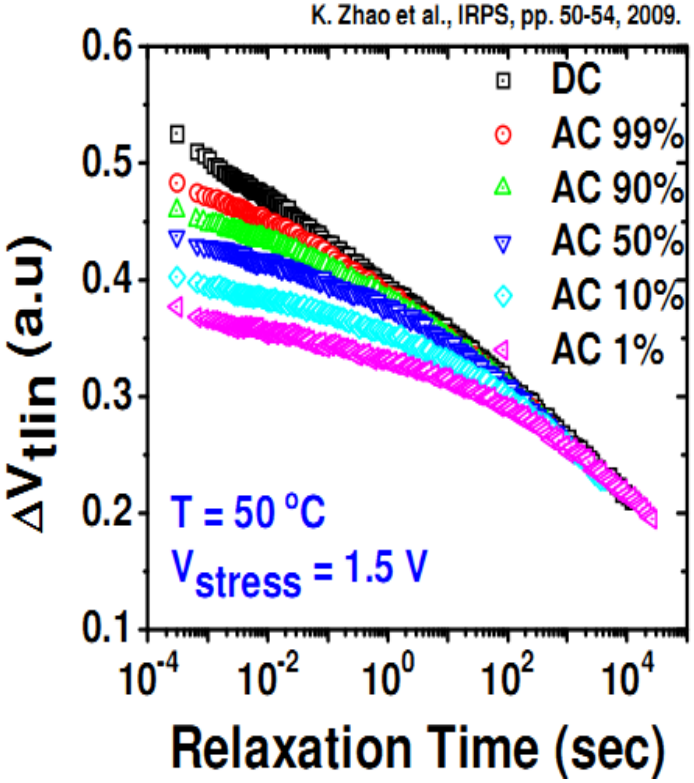


Example of PBTI Relaxation => Fast measurement is required.

NBTI and PBTI (DC vs. AC stress)

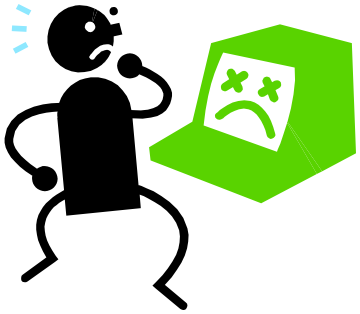
Impact of Stress Mode on PBTI Relaxation





Source: IRPS 2011 MG HK Tutorial

Our Customers' Problems



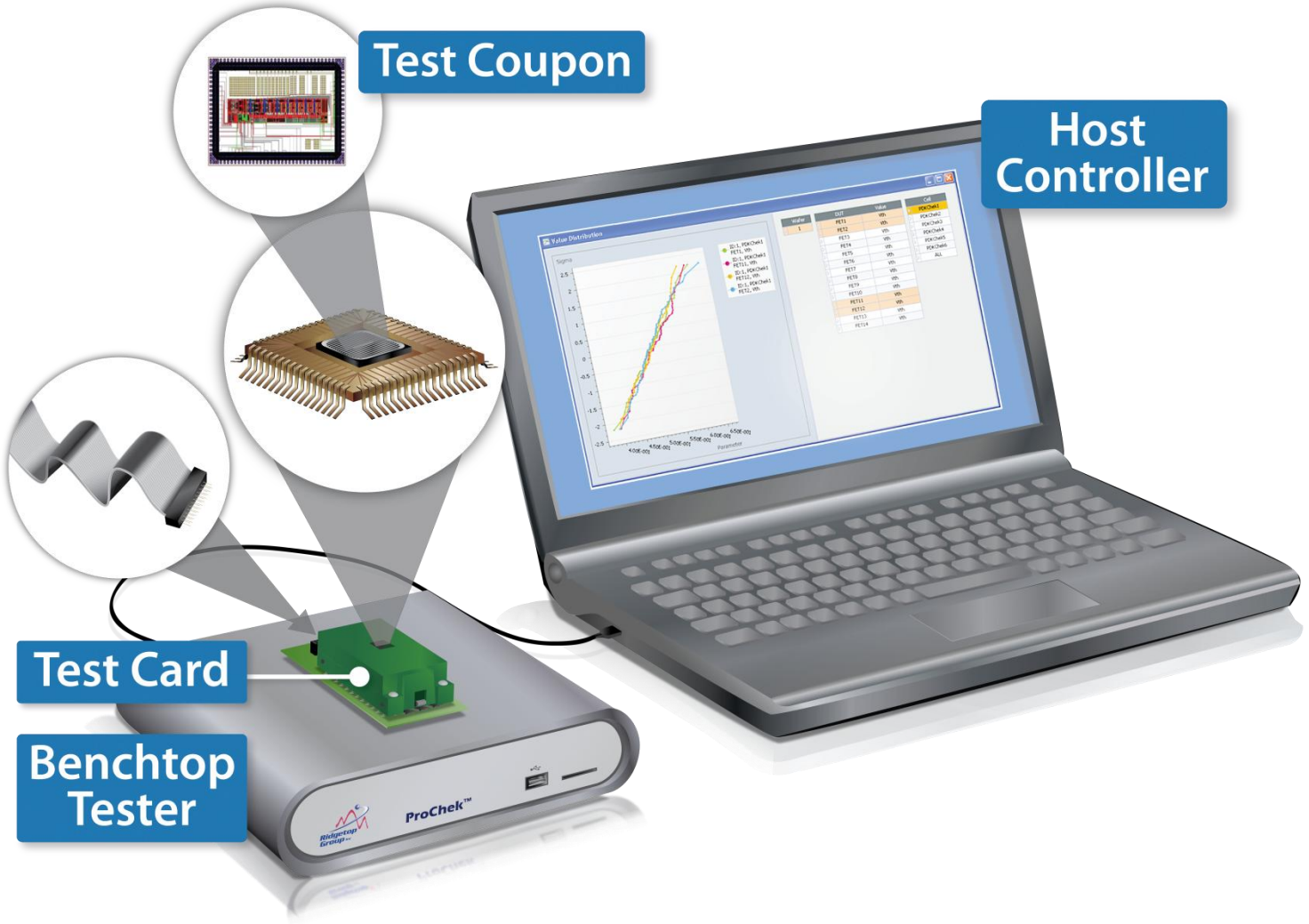
Customer 1:
"Foundries do not give us enough reliability test data"

Customer 2:
"We can test only three DUTs in parallel and the test lasts a full month"

Overview of the Existing Problem

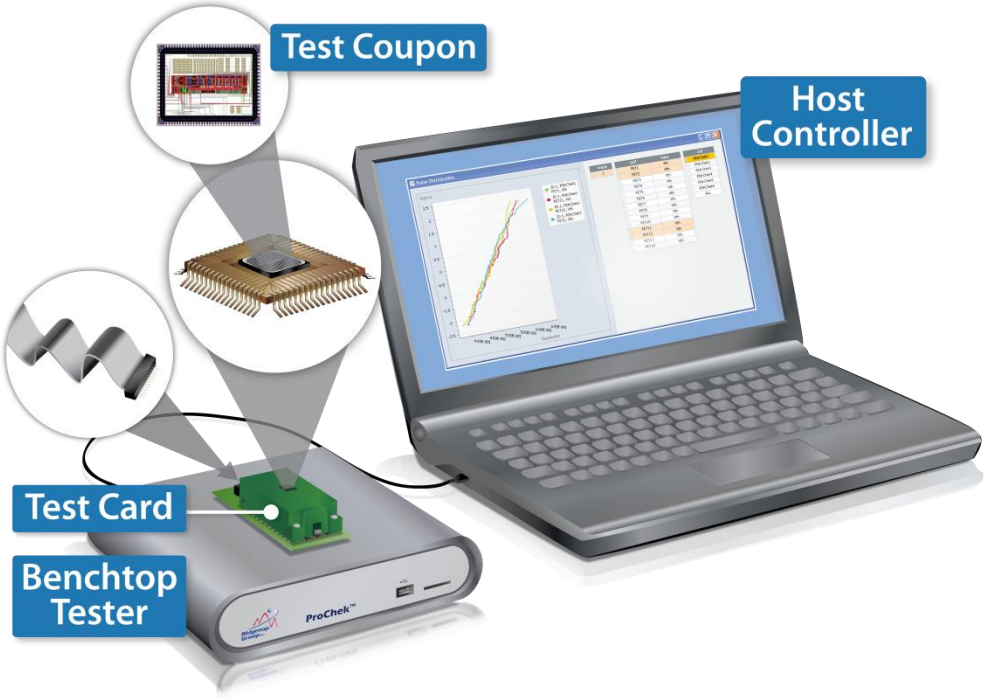
- Small-geometry fabrication processes are very complex
- Reliability concerns for demanding applications include:
  - Bias Temperature Instabilities
  - Dielectric Breakdown
  - Hot Carrier Effects
  - Electromigration
  - Stress Migration
  - Process Mismatch Effects
  - Lot-to-lot Variation
- For space and radiation-sensitive applications there are also:
  - Single-event radiation effects
  - Total dose radiation effects
- Current techniques are not:
  - Comprehensive enough
  - Accurate enough
  - Fast enough

Solution: ProChek *(Process Checker)*



What is ProChek?

ProChek is an innovative low-cost technique to very rapidly characterize the intrinsic reliability of deep submicron nanotechnology CMOS processes (bulk CMOS, SOI and SiGe)



Characteristics of ProChek

- Targets bulk CMOS, SOI, SiGe reliability concerns
  - NBTI / PBTI, TDDB, HC, EM, SM, TID
- Test Coupon
  - As little as 1 * 1 mm chip area
  - MPW for lower cost
  - 32 – 1024 devices can be tested in parallel for maximum throughput
  - On-chip per transistor heaters to 325 C, greatly reducing test time
  - Synthesizable (except for on-chip heaters) to speed deployment
- Benchtop Tester
  - Fully programmable test conditions cover DC and AC stress cases
  - Portable and compact
  - ATE not needed
- Host Controller
  - Easy-to-use software GUI
  - Rich suite of built-in reliability test templates
  - Data processing capabilities

Structure of ProChek

- Test Type
- Test Bias
- Test Duration
- Result Collection
- Result Processing

HOST CONTROLLER + GUI

BENCHTOP TESTER

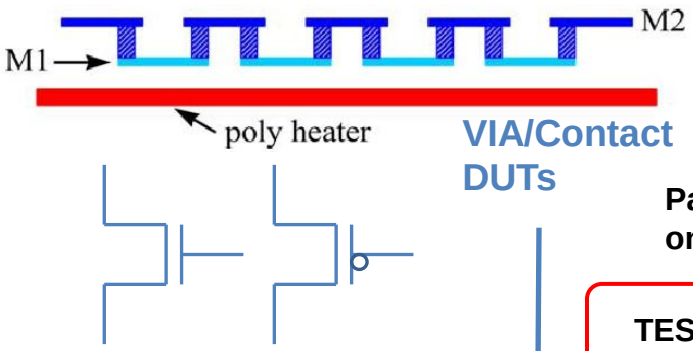
USB 2.0

RAM

MCU

Programmable sources

Prog. sources and I/V meas. devices



VIA/Contact DUTs

Packaged chip on Test Card

TEST COUPON

Transistor DUTs

Address Logic

DUTs

DUTs

DUTs

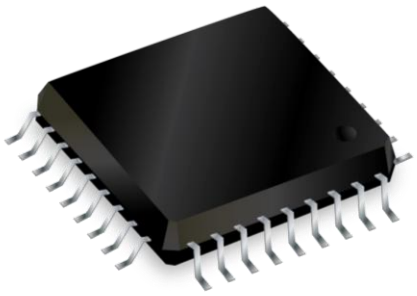
DUTs

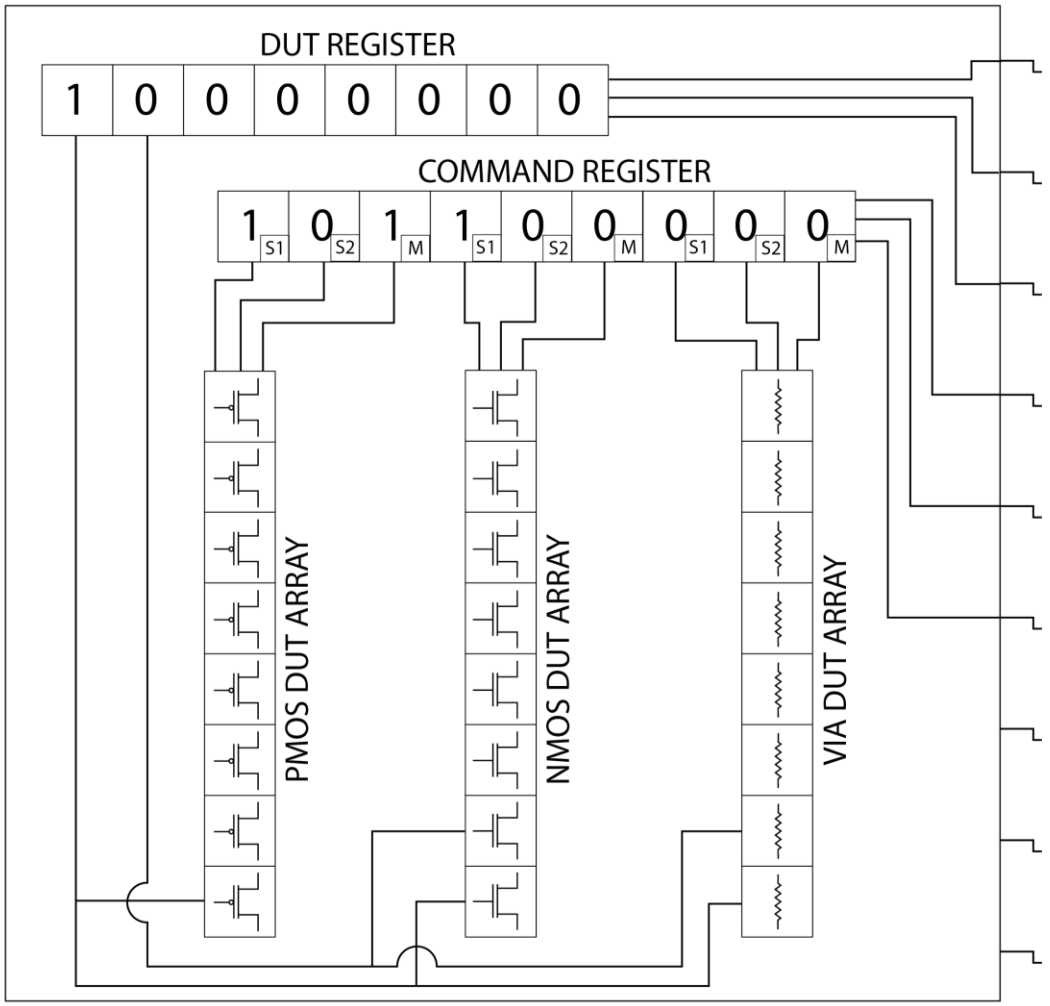
V_S (0 – 5V, 0 – 1 MHz)

V_M (0 – 5V, 100 pA)

16 X 64 DUTs …or more

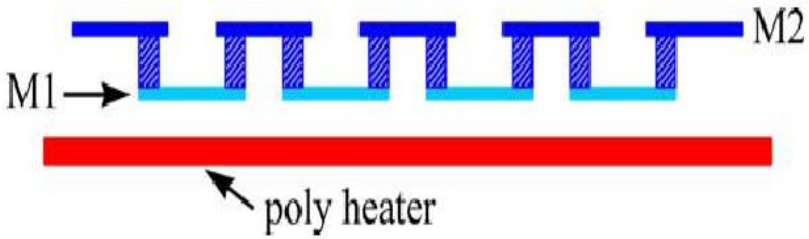
Test Coupon Chip



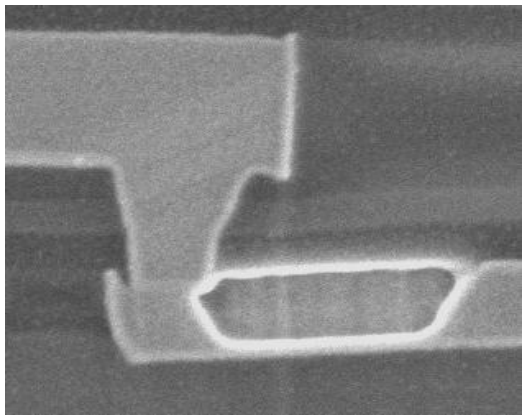


The Test Coupon is a packaged chip that contains arrays of DUTs that are addressed from serial package pins and stressed and measured with the high-resolution Benchtop Tester.

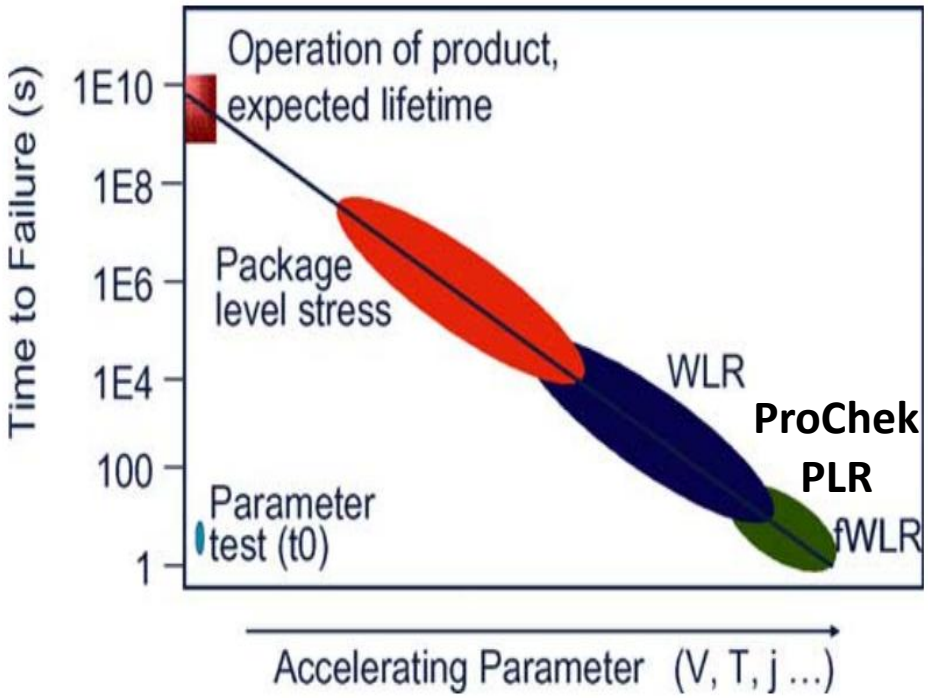
Test Coupon Chip: Local Heating Structures



Local poly-silicon heaters capable of 325 ˚C will reduce EM, SM and BTI test time and cost

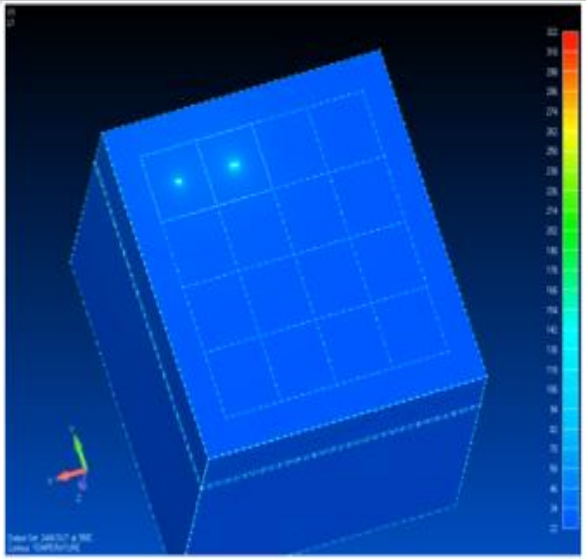


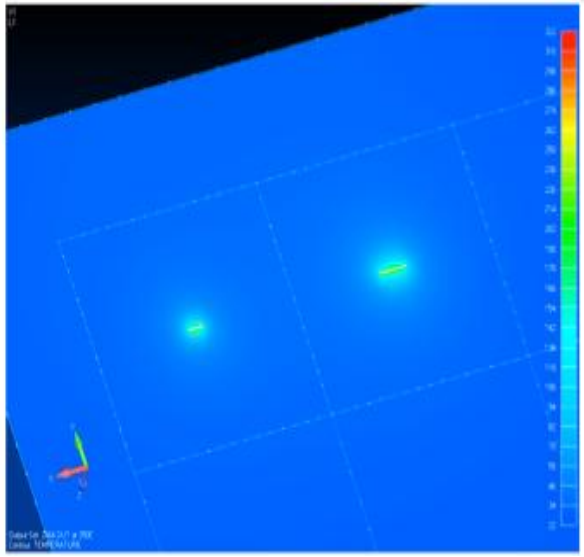
EM-induced void



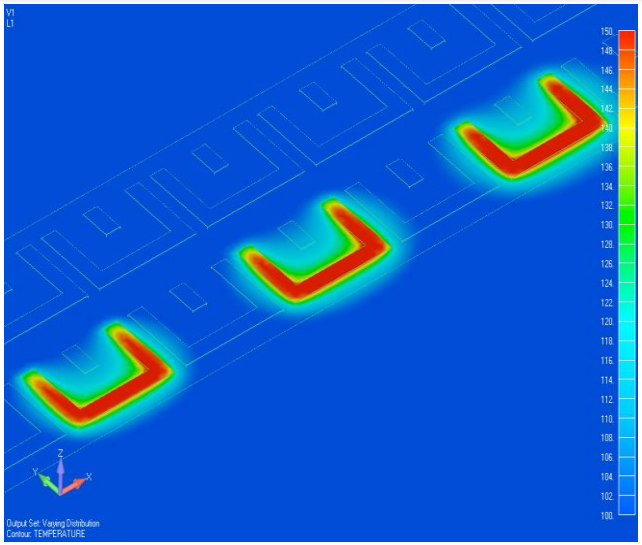
With robust on-chip circuitry and local heaters, ProChek provides as high acceleration factor for package level reliability testing (PLR) on parallel DUTs as currently done for single DUTs in fast Wafer Level Reliability Testing (fWLR).

Thermal Simulation Results





Two heated DUT arrays are shown on a 2 mm^2 (packaged) chip



Device-level zoom-in

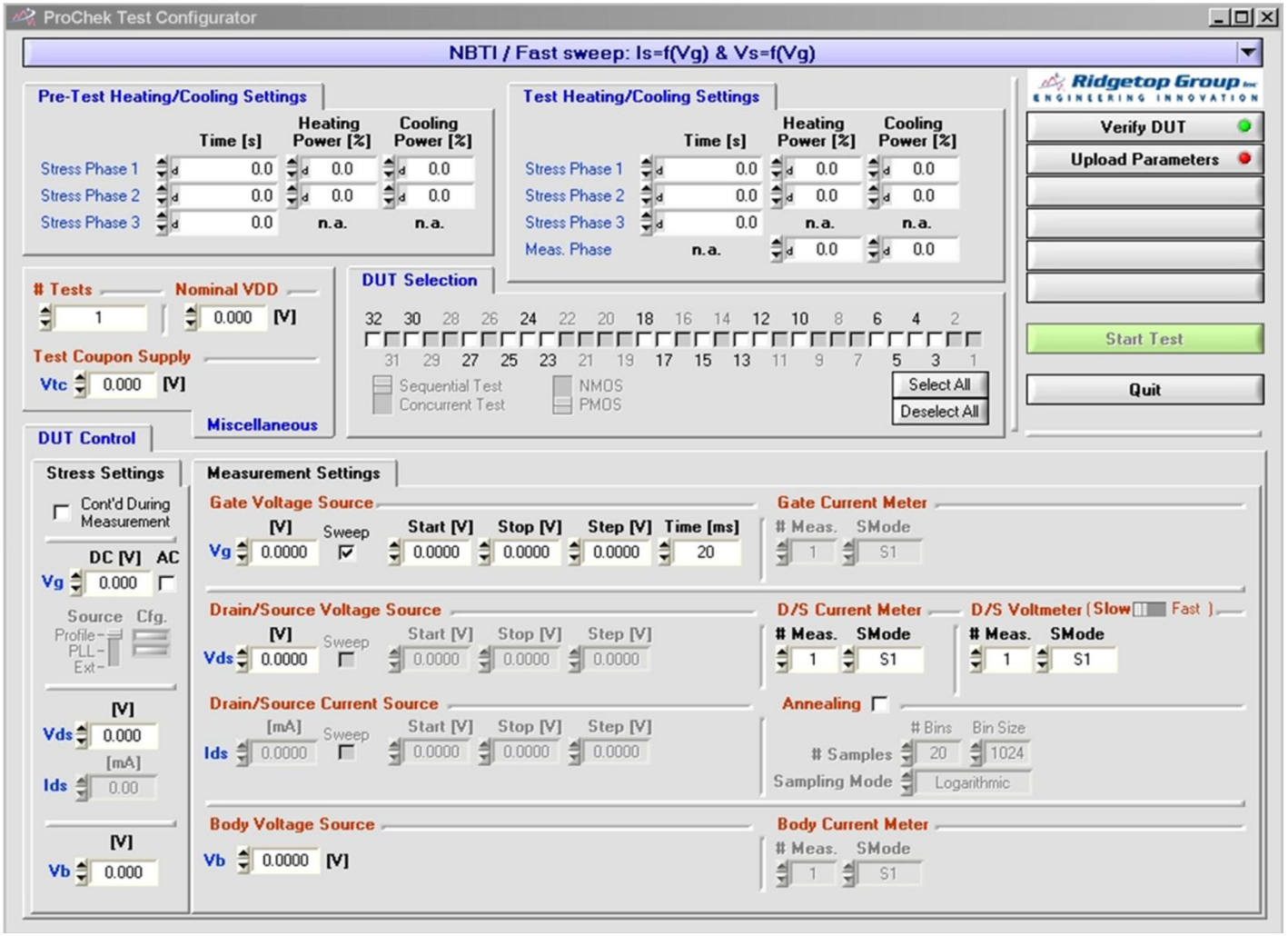
Temperature scale varies from 322 to 22 °C

According to 3D thermal simulations, the localized DUT arrays heat up to 325 °C in 75 milliseconds and consume 16 mW of power per DUT during the test. The temperature drops rapidly on the chip, so the non-stressed structures will not undergo any damage.

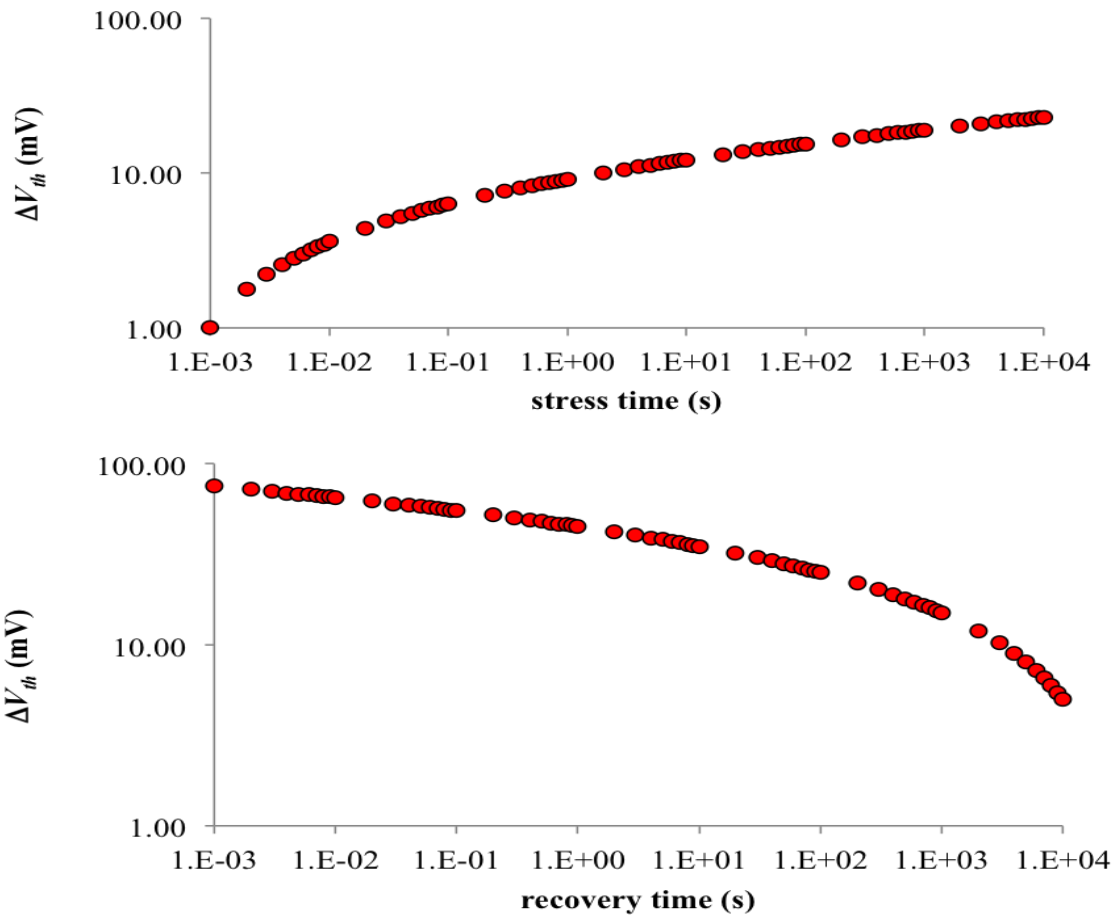
ProChek GUI

Measurement templates include:

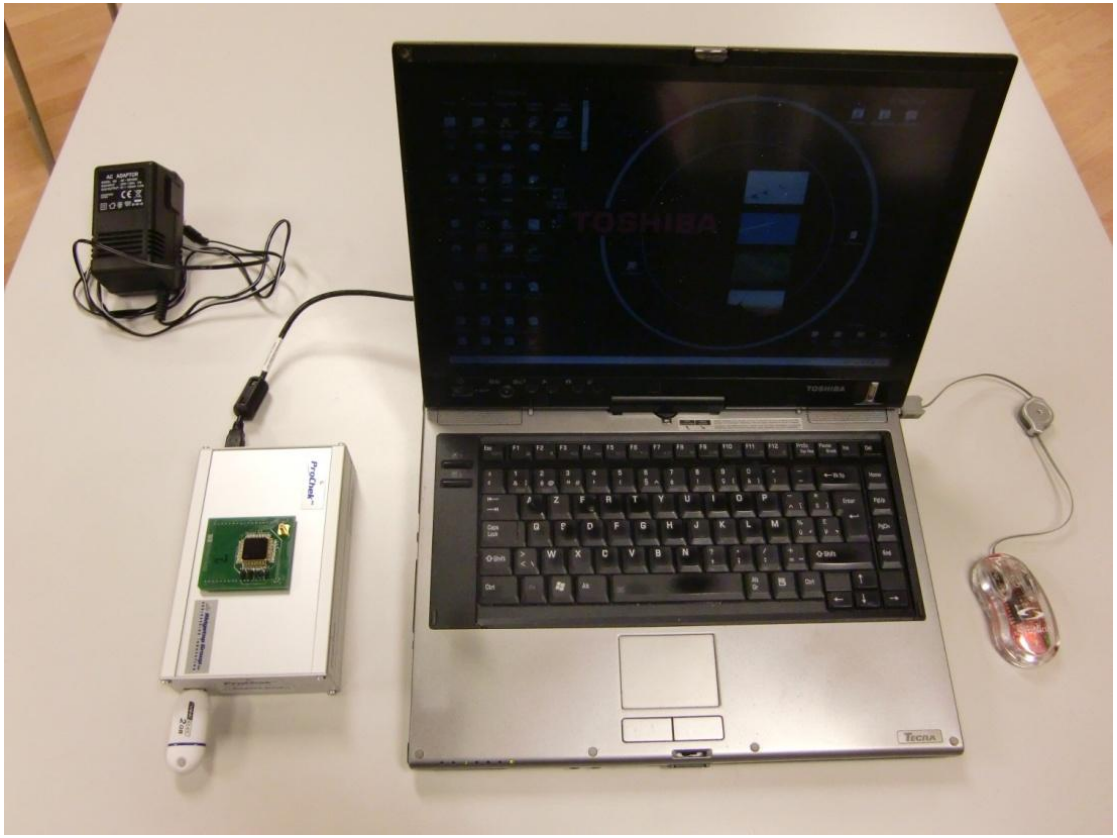
- QBD
- TDDB
- HCI / V_T Shift
- HCI / Fast Sweep
- HCI / Slow sweep
- PBTI / V_T Shift
- PBTI / Fast Sweep
- PBTI / Slow Sweep
- NBTI / V_T Shift
- NBTI / Fast Sweep
- NBTI / Slow Sweep
- TID
- Via (Electromigration, Stress Migration)



ProChek GUI: BTI Test

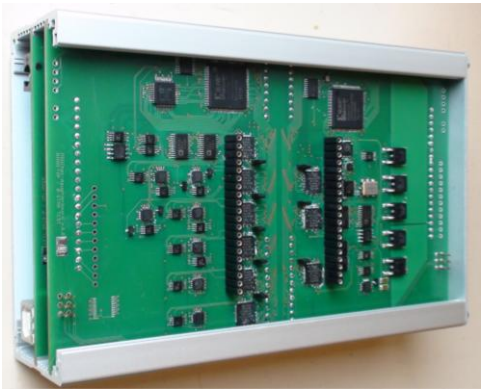
BTI test:	Example (from analytical calculations, not measured):
Example of basic on-the-fly (OTF) measurement: • Drain current is monitored during a single stress and a single relaxation phase. • During stress: Vg = 0, Vs = Vb = Vstress, Vd = Vstress – 50 mV. Measure I_d 10 times per decade (logarithmic sampling rate), starting from 10^{-3} s stopping at 10^4 s • During relaxation: $V_g \approx V_{stress} - \lvert V_{th0} \rvert$, $V_s = V_b = V_{stress}$, $V_d = V_{stress} - 50$ mV (measure in subthreshold). Again, measure I_d 10 times per decade (logarithmic sampling rate), starting from 10^{-3} s after removing the stress and stopping at 10^4 s.	

ProChek Benchtop Tester

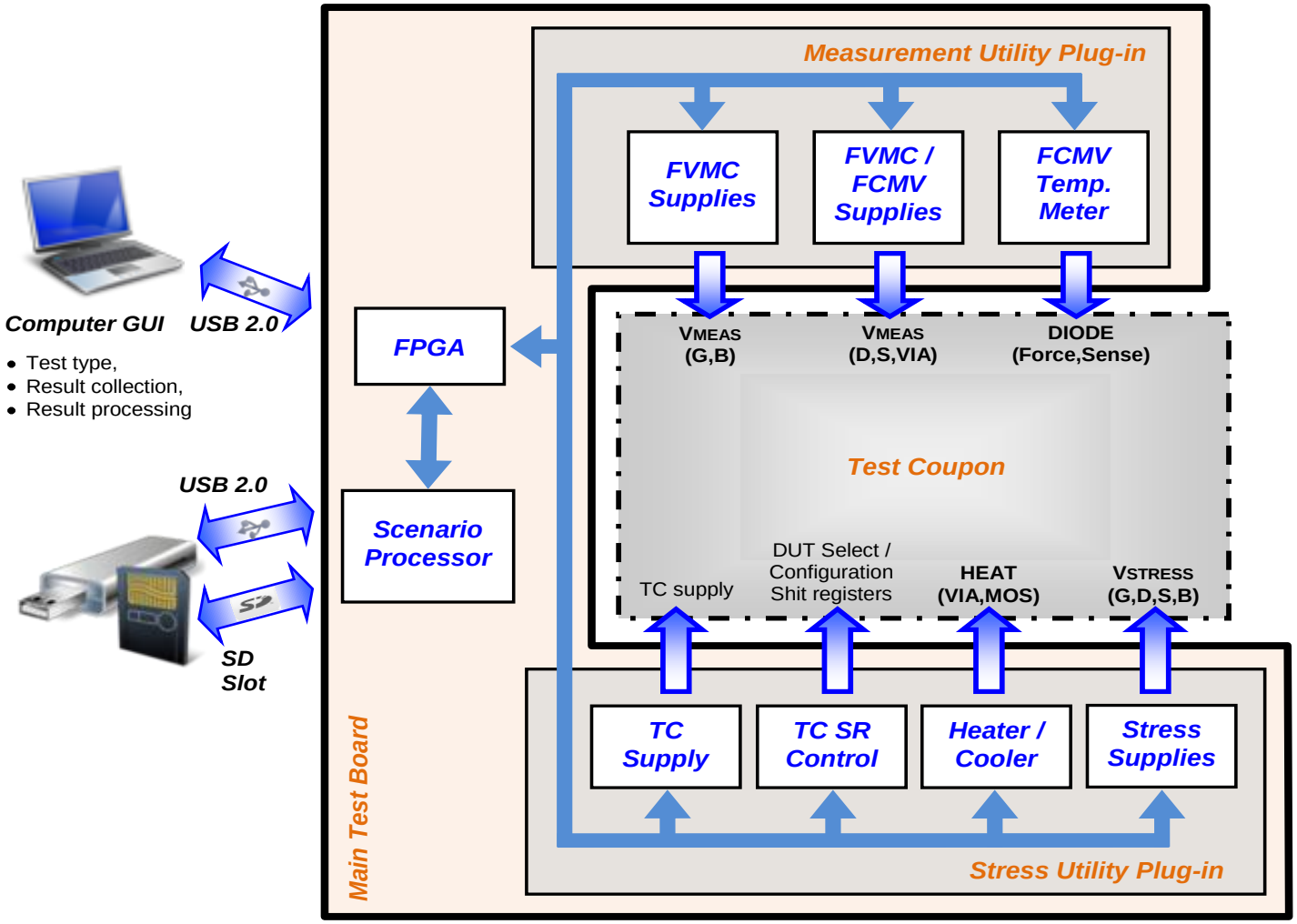


ProChek Benchtop Tester connected to a laptop

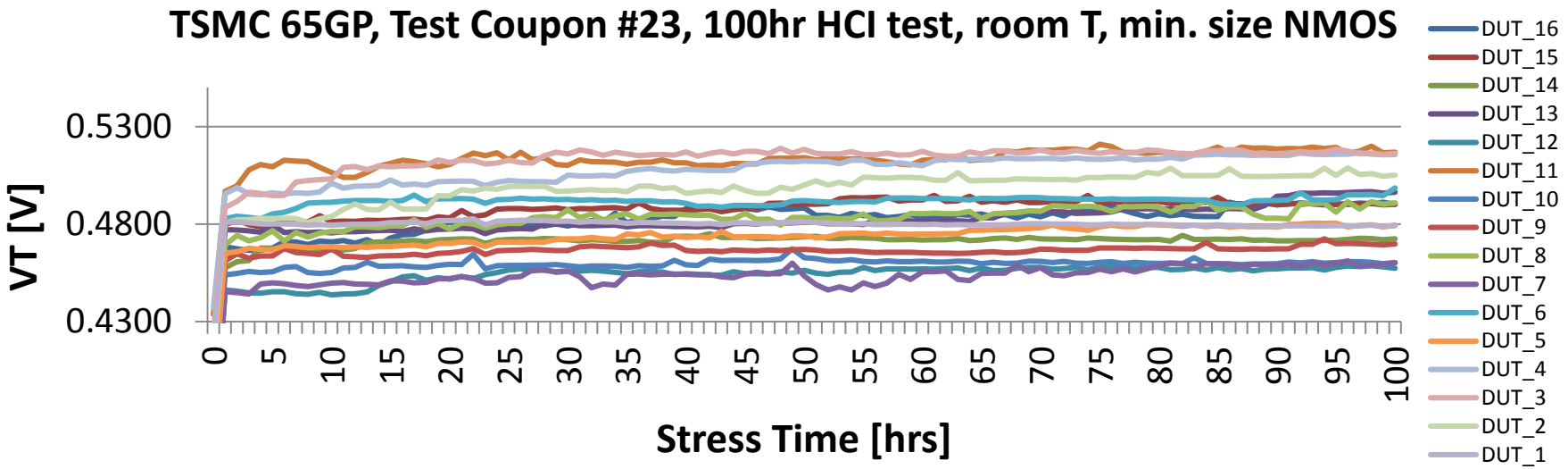
Circuit boards inside the ProChek Benchtop Tester

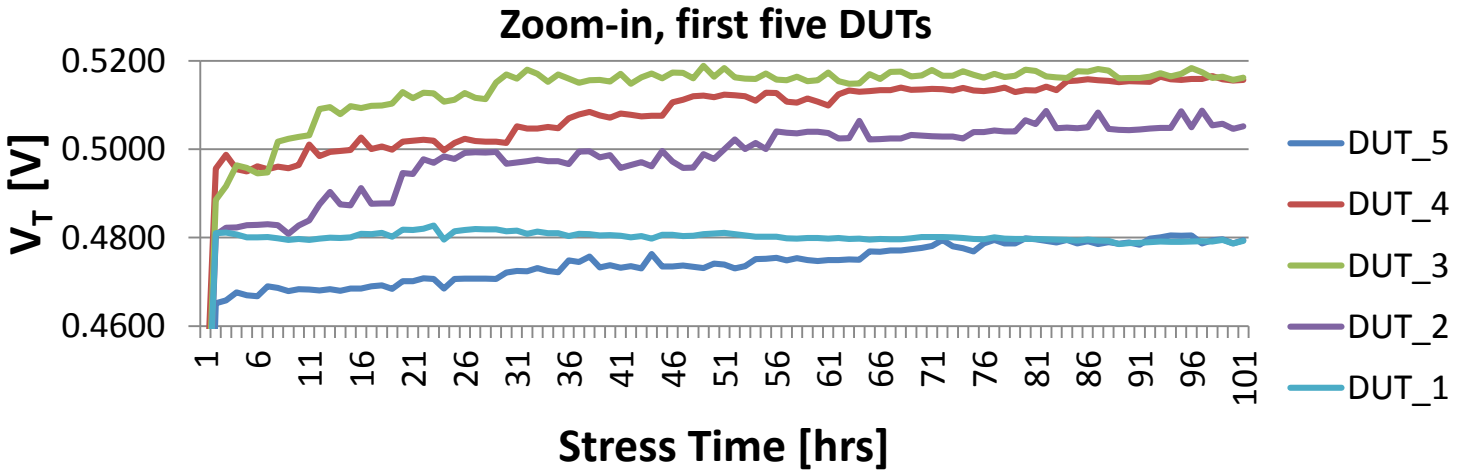


Benchtop Tester Architecture

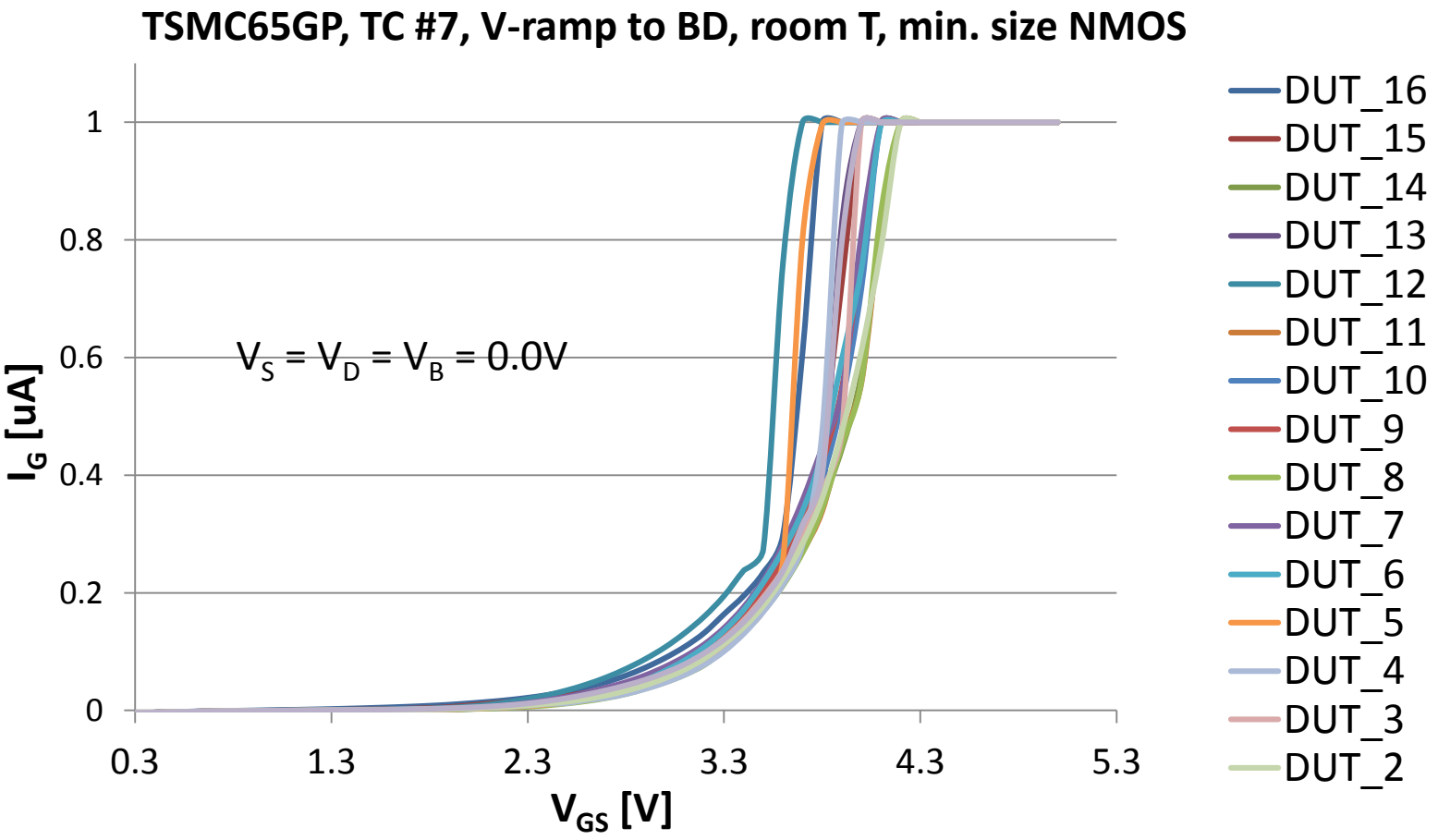


ProChek Test Results: Hot Carrier

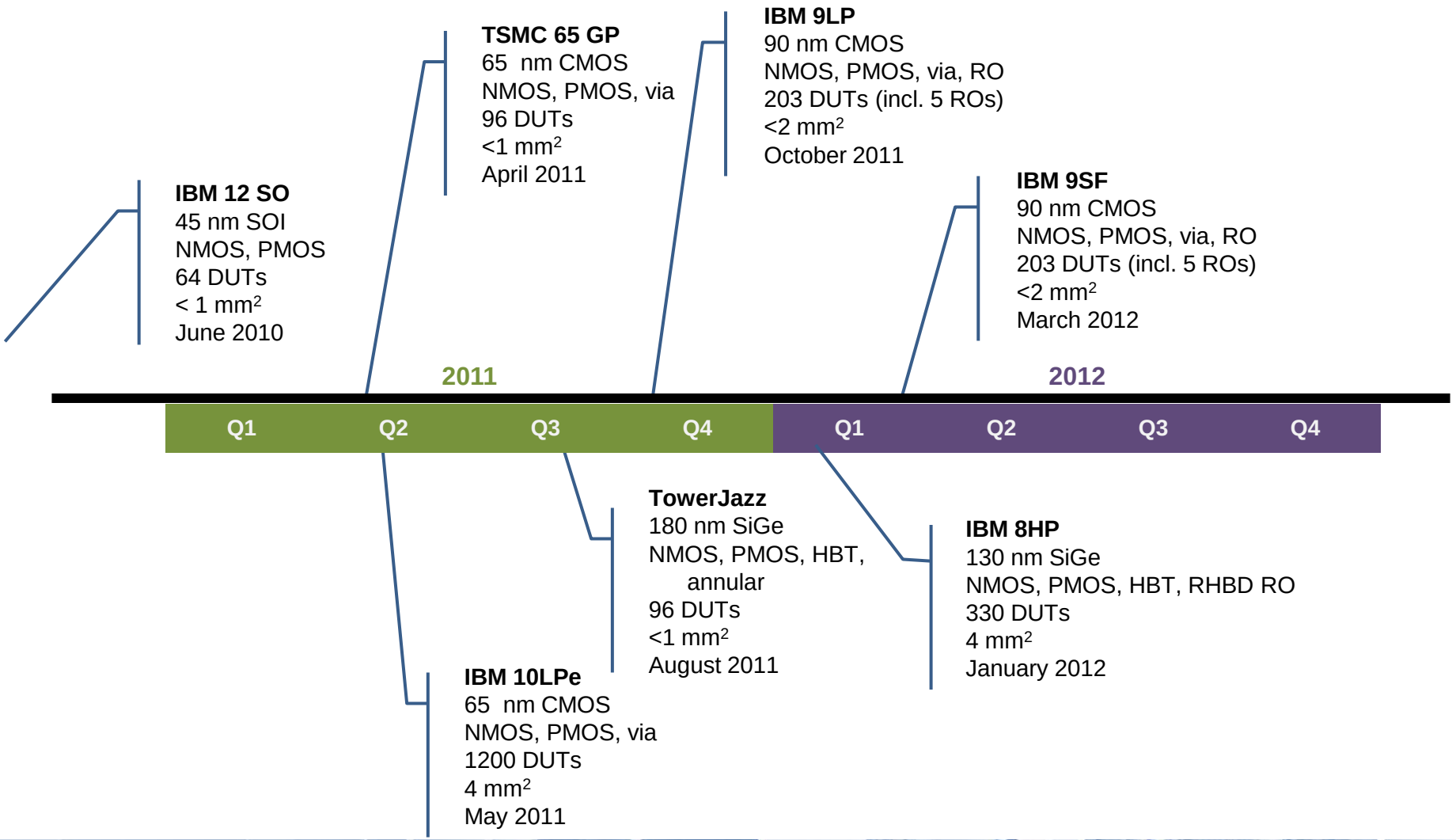




ProChek Test Results: V-ramp to Breakdown



ProChek Test Coupons: Targeted Processes



Summary

- ProChek is an advanced new tool for fabrication process qualification that offers significant advantage to IC designers and reliability engineers
  - Cost and time budgets of fabrication process qualification are significantly reduced
  - Covers (all) the reliability concerns of modern nanotechnology processes

Questions?

Upcoming Webinars

Ridgetop Group Inc
ENGINEERING INNOVATION

Topic	Date	Time
Implementation of Prognostics in Solar Applications	Wed. Jun 27, 2012	1:00 - 2:00 PM PDT
Troubleshooting Analysis and Decision Support in Complex Applications	Wed. Jul 25, 2012	1:00 - 2:00 PM PDT

For more information about Ridgetop Group Webinars, email us at information@ridgetopgroup.com

Thank you!

Ridgetop Group, Inc.

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