
ProChek™

# The Shortcut to Device and Process Qualification, Characterization, Comparison and Reliability Assessment.

Hans Manhaeve, Ph.D.

July 9, 2014

# Agenda

- The Quest for Data – Setting the Scene
- Brief History of ICs
- Aspects of IC Reliability
- Degradation Mechanisms of Modern CMOS ICs
- ProChek Concepts
  - Structure and Specs
  - Test Coupon IP
  - GUI
  - Benchtop Tester
  - Targeted Fabrication Processes and Test Results
- Summary

# The Quest for Data

## Macro Issues

- Semiconductor industry business is based on a fabless model
- Foundries share only a limited amount of process information
- Smaller semiconductor structures have relatively more variability in critical process parameters
- Speed and frequency of process changes increases
- Wafer Level Process Monitors have limited statistical significance
- Customers expect ZERO defects on shipped products

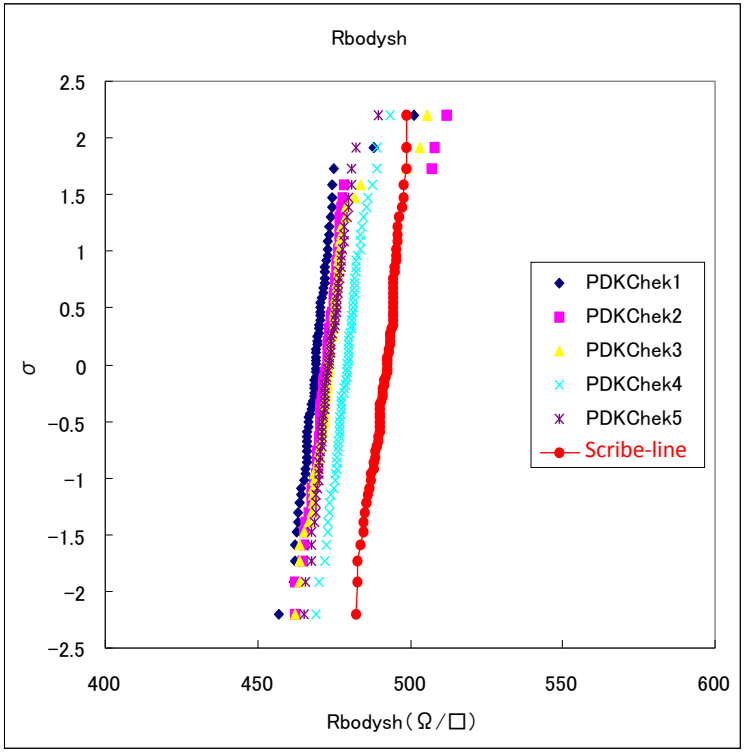
## PDK Gaps

- PDK may not be accurate for particular batch/wafer/die/package
- PDK may not have data for particular application (e.g., temp.)
- PDK may not be representative of particular biasing schemes (e.g., MOSFET matching differs for strong inversion and subthreshold)
- Data is not placement specific (proximity/wafer angle)
- PDK may not give values to insert into random parameter fluctuation simulations

In an increasingly cost-conscious and price sensitive landscape, yield loss damage is magnified

# The Quest for Data

- Process control monitor (PCM) structures from foundry may not directly measure important parameters
- High performance designs need die-level process monitor (DLPM) results that accurately track actual process tuning




Scribe-line results differ from DLPM results

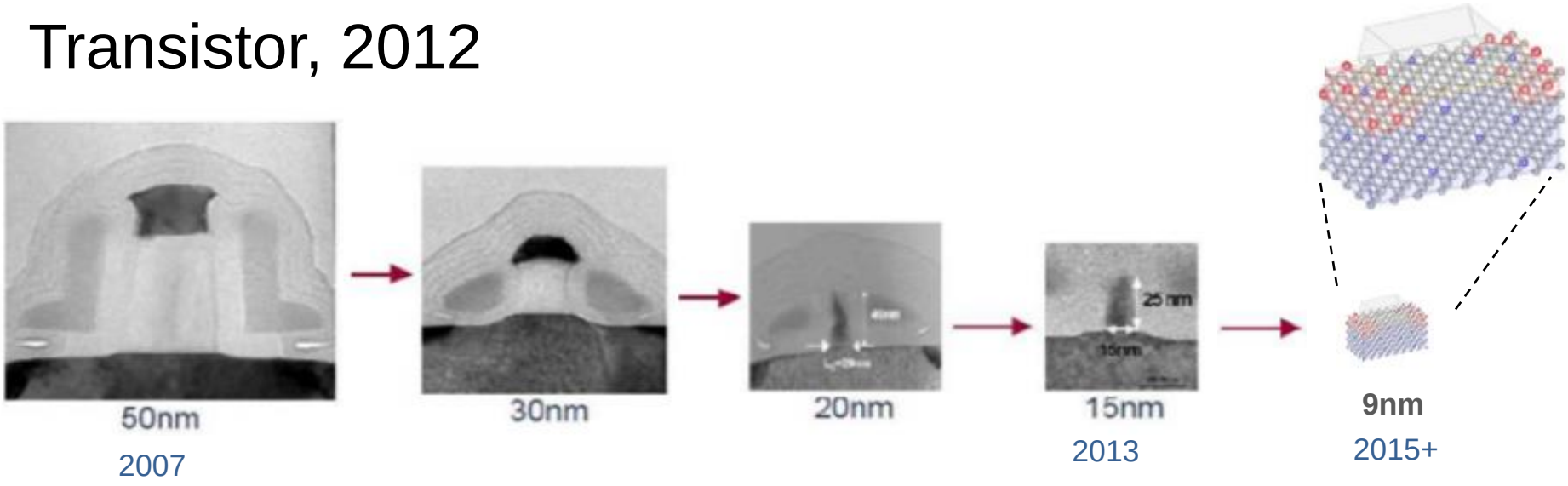
# History of Integrated Circuits

## First transistor, 1947

Size: 10 cm
Speed: Slow
Circuit Density: 0.0001 devices per 1 $mm^2$

# History of Integrated Circuits

## Transistor, 2012

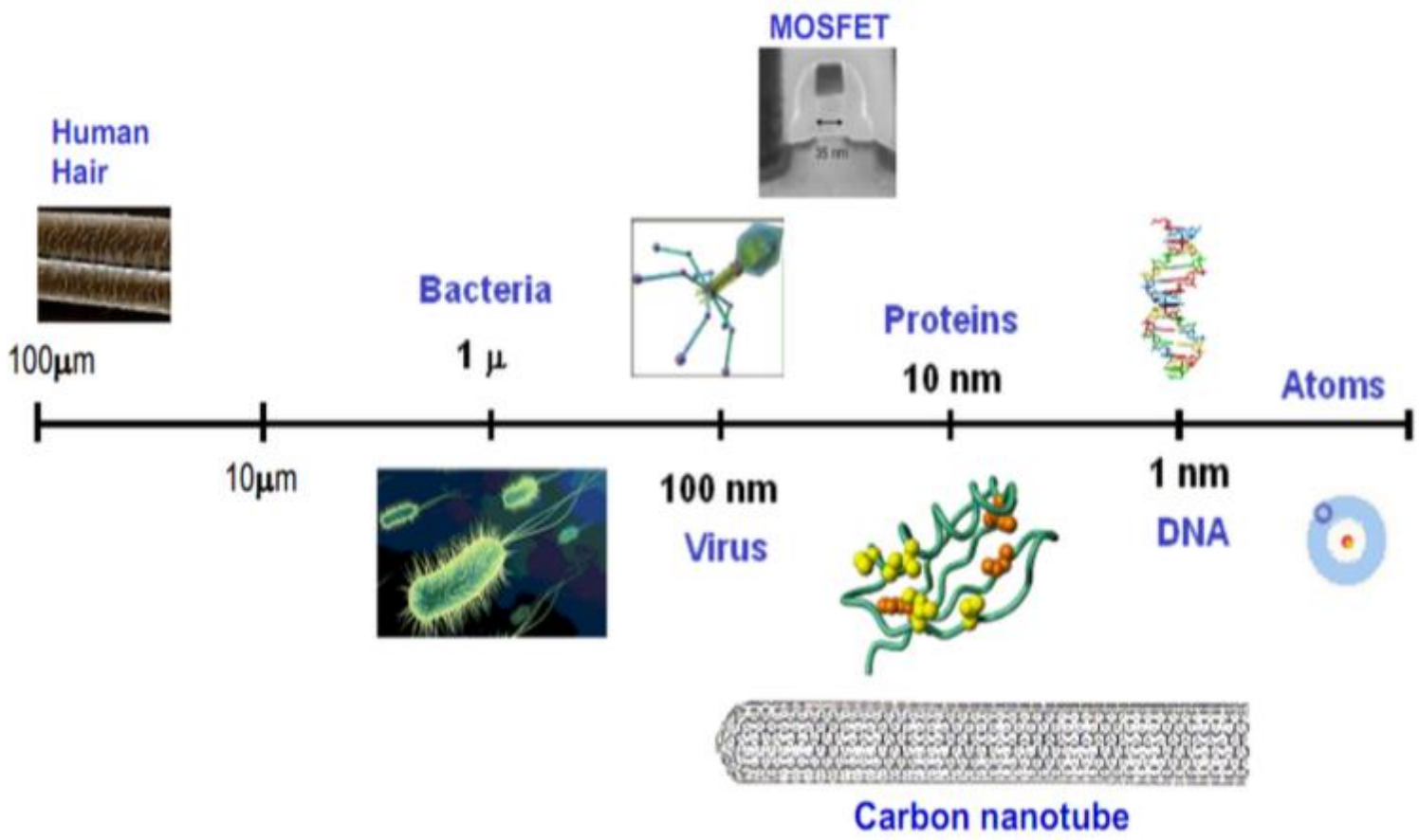



Size: 14 nm
Speed: >500 GHz
Circuit Density: 50,000,000 devices per 1 $mm^2$

500,000,000,000X improvement in circuit density in 65 years!

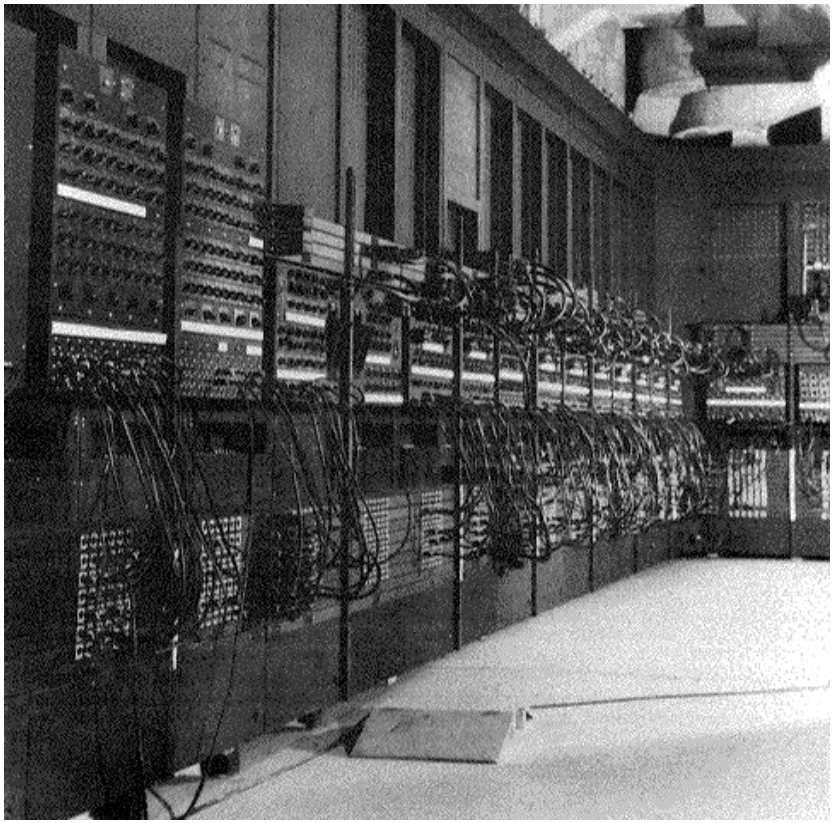
# History of Integrated Circuits

Size comparison, 35 nm MOSFET shown



# History of Integrated Circuits

First “super computer,” 1947
(ENIAC, “the Giant Brain”)

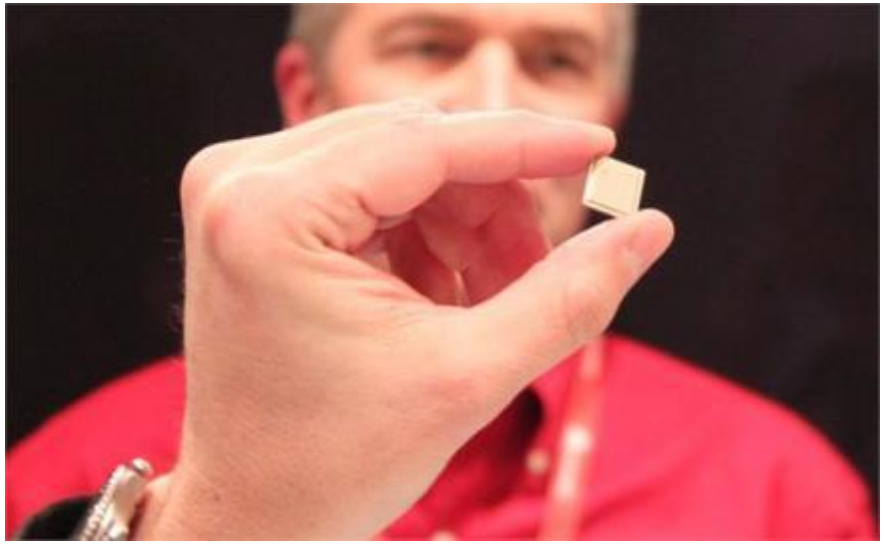


Size: 1800 square feet
Performance: 5,000 FLOPS
Power: 150 kW
Reliability: >10 years

“Where a calculator on the ENIAC is equipped with 18,000 vacuum tubes and weighs 30 tons, computers of the future may have only 1,000 vacuum tubes and perhaps weigh 1½ tons.” – *Popular Mechanics, March 1949.*

# History of Integrated Circuits

## Microprocessor 2012



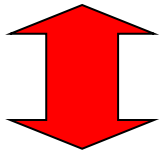
Size: 200 $mm^2$
Performance: 1,000,000,000,000 FLOPS
Power: 100 W
Reliability: 10 years **???**

300,000,000,000X improvement in wattage/FLOP in 65 years!

How about reliability?

# Yield & Reliability

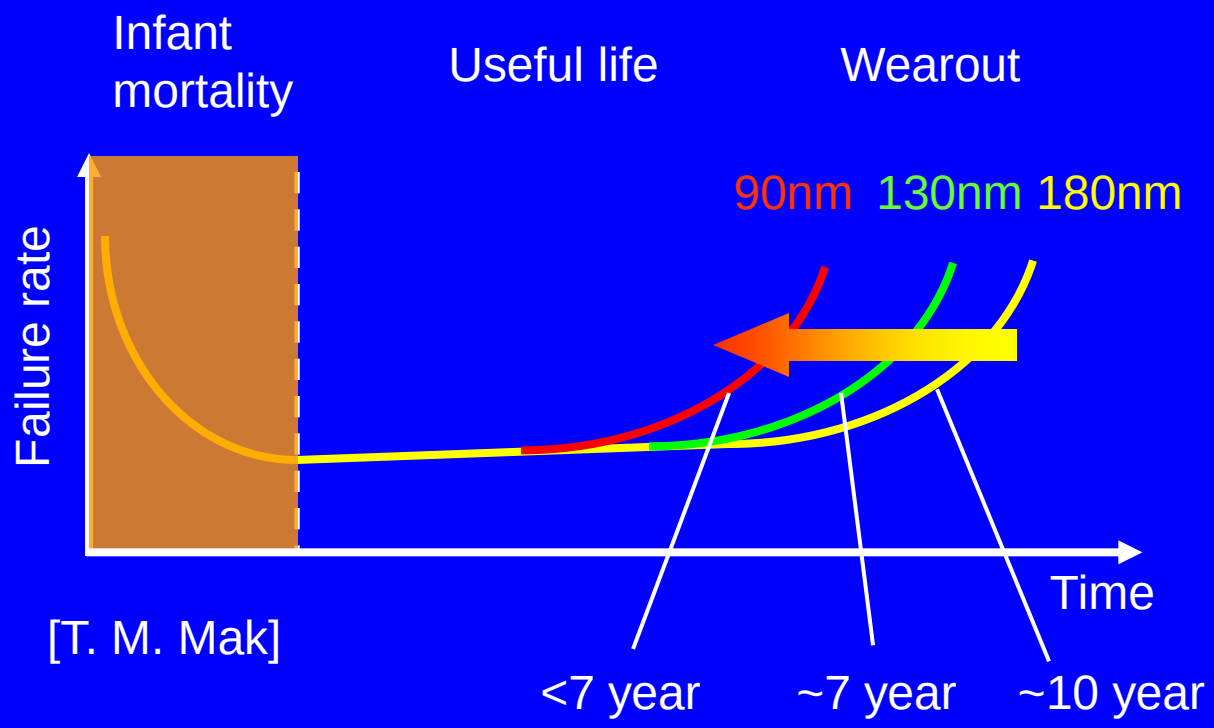
- Semiconductor evolution enables further integration
  - Transistors are nearly for free
- New processes are used for mass production long before they are mature
  - Systematic and random defects
  - Reliability concerns
- Increasing device complexity
  - The “embedded” world
  - Analog – Digital – Memory – Software



- Market demands for cheaper and better electronics
- Market demands for RELIABLE electronics

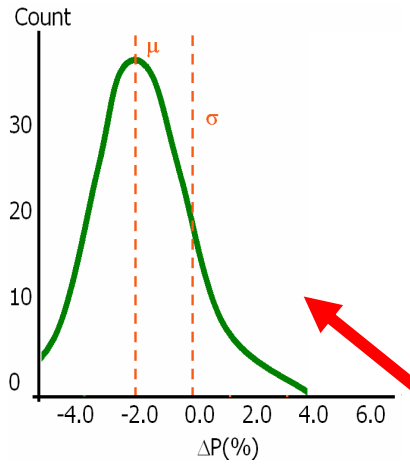
# Aspects of IC Reliability

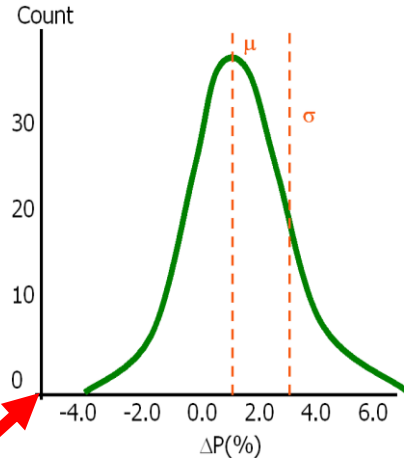
## IC lifetime is becoming a serious concern

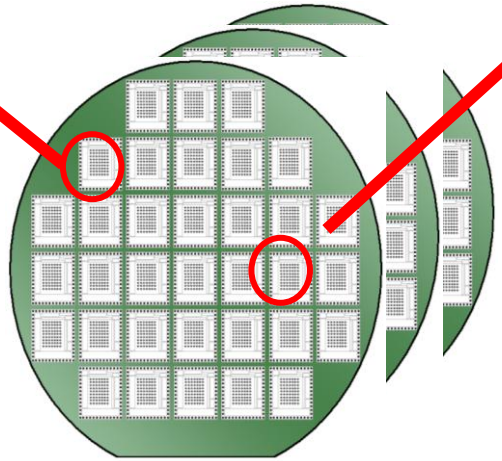


# Need for proper process characterization

## Dealing with variance and fluctuations



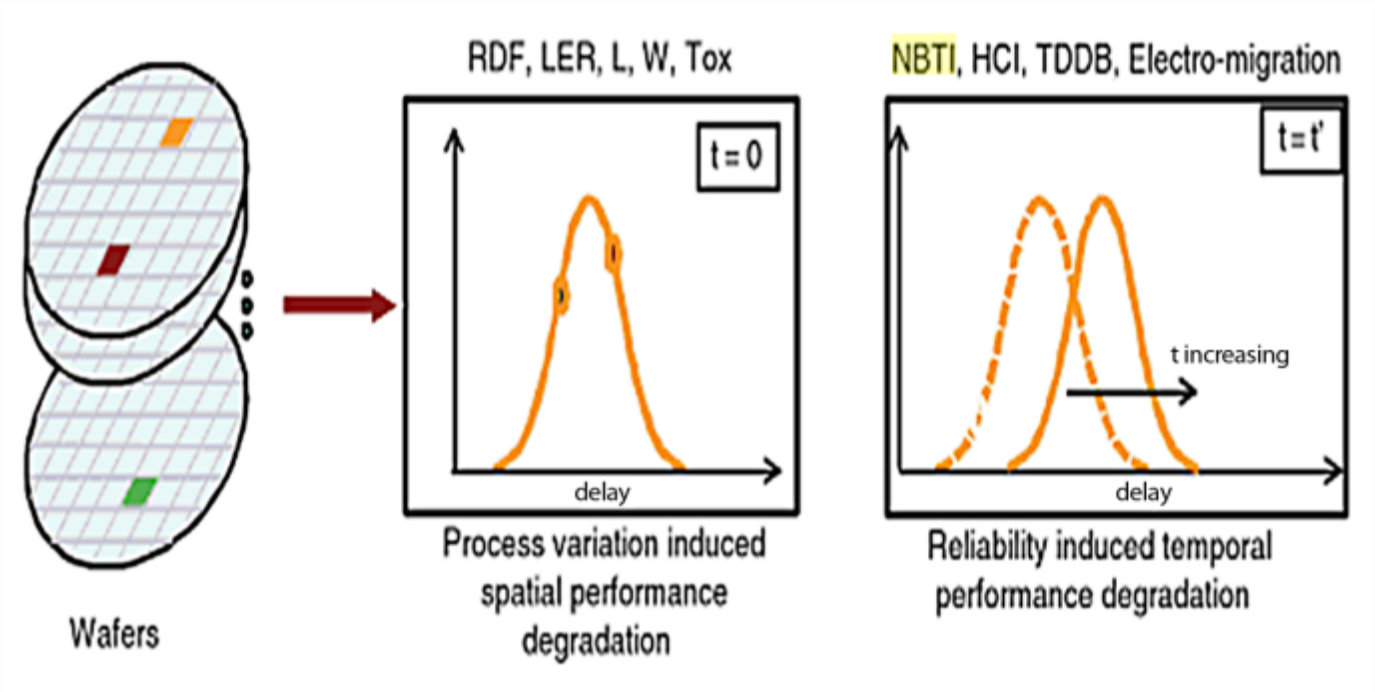



**Parameters change across dies, across wafers and across lots**

**PDK provides the boundaries**

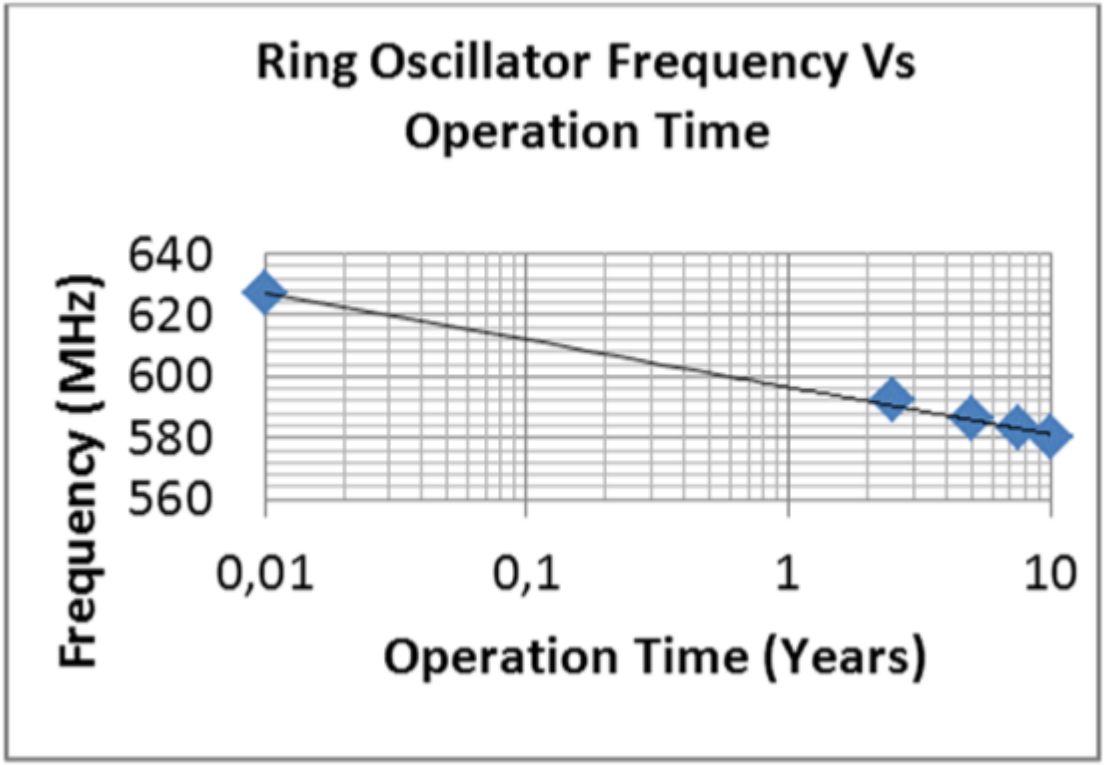
# Variability: Impact on Reliability




Time-zero parameter spread due to process mismatch shifts during the operational life due to degradation. Both process mismatch and degradation effects are worse in the smallest-geometry processes.

Source: “Low-Power Variation-Tolerant Design in Nanometer Silicon” By Swarup Bhunia

# Aspects of IC Reliability




28 nm CMOS ring oscillator frequency degrades 5.5% within a year in normal operation conditions

Source: Synopsys

# Cost of Reliability Problems

B-2 bomber crash in Guam Feb 2008.

- $1.4B loss

Moisture in the transducers during calibration distorted the information in the air data system.

This caused the flight control computers to calculate inaccurate airspeed and negative angle of attack upon takeoff.

http://telstarlogistics.typepad.com/telstarlogistics/2008/08/photos-and-vide.html

# Cost of Reliability Problems

SANTA CLARA, Calif., Jan. 31, 2011 – As part of ongoing quality assurance, Intel Corporation has discovered a design issue in a recently released support chip, the Intel® 6 Series, code-named Cougar Point, and has implemented a silicon fix. In some cases, the Serial-ATA (SATA) ports within the chipsets may degrade over time, potentially impacting the performance or functionality of SATA-linked devices such as hard disk drives and DVD-drives. The chipset is utilized in PCs with Intel's latest Second Generation Intel Core processors, code-named Sandy Bridge. … Intel expects this issue to reduce revenue by approximately **$300 million** as the company discontinues production of the current version of the chipset and begins manufacturing the new version. Full-year revenue is not expected to be materially affected by the issue. Total cost to repair and replace affected materials and systems in the market is estimated to be **$700 million**.

Source: Intel Newsroom

# Degradation Effects: Overview

| Failure Mode | Physics | System Effect |
|---|---|---|
| NBTI (PMOS), PBTI (NMOS) | ▪ Negative $V_T$ shift for PMOS, positive for NMOS<br>▪ Lower leakage and $I_{ON}$, slower speed | ▪ Timing faults in processors other digital circuits<br>▪ Resettable – but increasing severity over time |
| TDDB | ▪ Soft breakdown:<br>  ▪ Slower speed<br>  ▪ Weakened gate oxide<br>  ▪ Increased leakage current | ▪ Increased ESD vulnerability<br>▪ Non-resettable timing faults |
| | ▪ Hard breakdown | ▪ Catastrophic short |
| Hot Carrier (NMOS) | ▪ Positive $V_T$ shift<br>▪ Change in sub-threshold swing (transistor won't turn OFF) | ▪ Increased Off-state power<br>▪ Increased current draw<br>▪ Decreased data retention time in DRAM |
| Metal Migration | ▪ Higher resistance in Via connections<br>▪ Open circuits | ▪ Catastrophic open |

# Failure Modes Impacting Reliability

- Via/metallization failure mechanisms
  - Electro migration
  - Stress migration
- Transistor failure mechanisms
  - Time-dependent dielectric breakdown (TDDB)
  - Hot carrier degradation
  - NBTI and PBTI

# Via/metallization Failure Mechanisms: Electromigration and Stress Migration

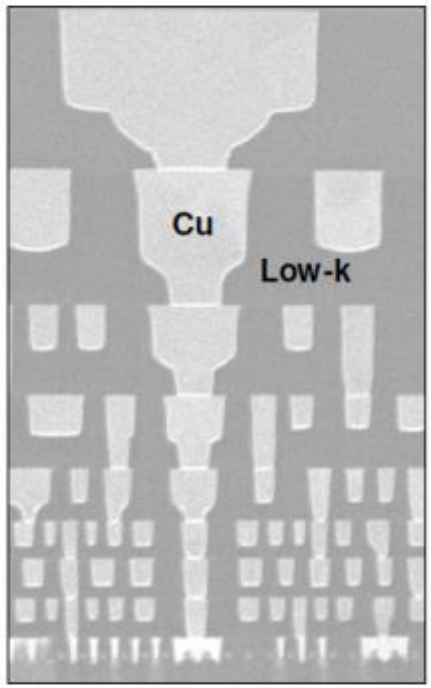
## 45 nm Interconnects

Loose pitch + thick metal on upper layers

- High speed global wires
- Low resistance power grid

Tight pitch on lower layers

- Maximum density for local interconnects



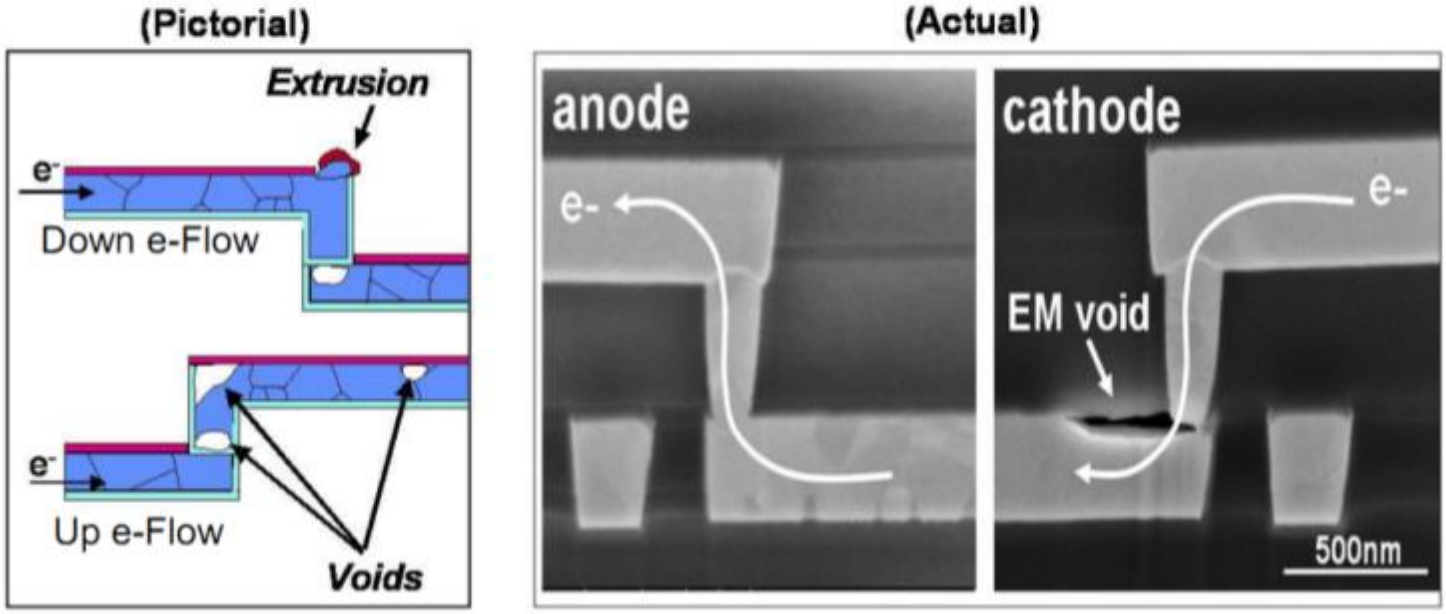

| | Pitch (nm) |
|---|---|
| M8 | 810 |
| M7 | 560 |
| M6 | 360 |
| M5 | 280 |
| M4 | 240 |
| M3 | 160 |
| M2 | 160 |
| M1 | 160 |

Hierarchical interconnect pitches

Modern CMOS processes have several metallization layers (up to a dozen).

# Degradation Mechanisms: Electromigration

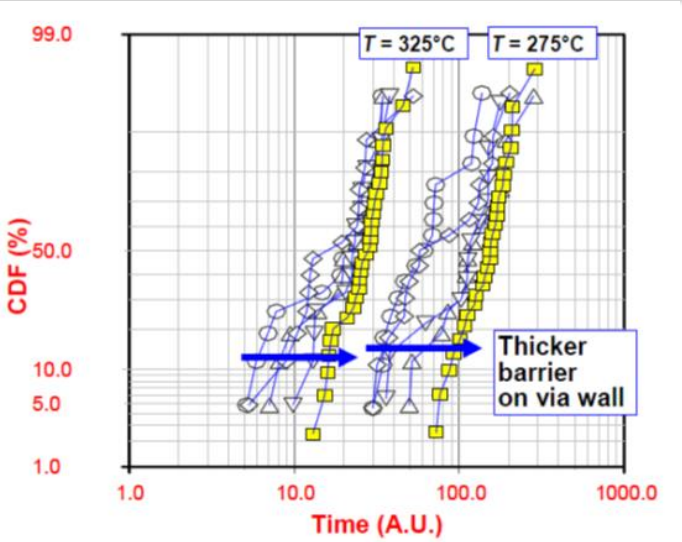
## Electromigration Associated with Vias

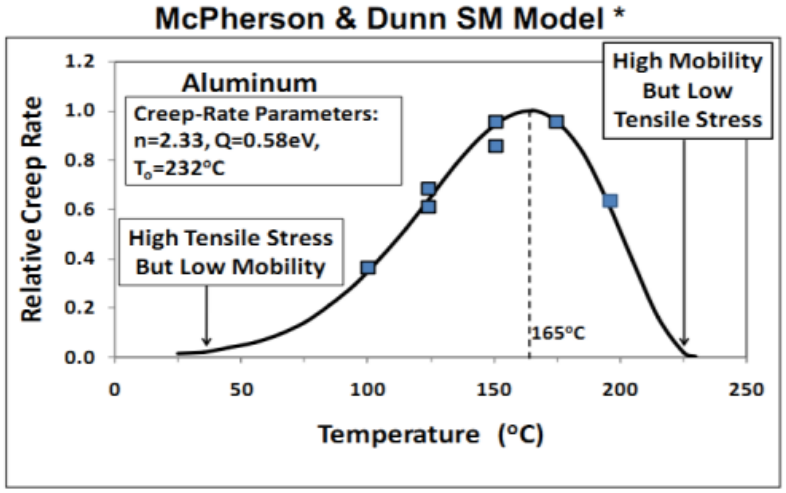


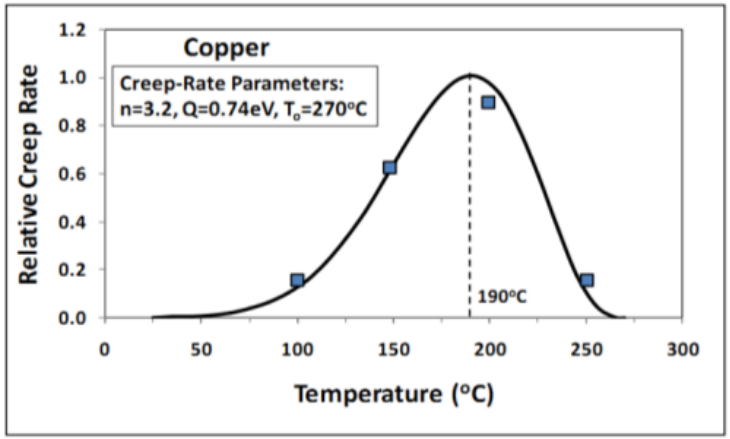

Source: IRPS 2011 Tutorials

# Electromigration & Temperature

- A 50°C increase in stress temperature decreases the EM test time with one order of magnitude
- Al stress migration/void rate peaks at 150-175 °C
- Cu stress migration/void rate peaks at 175-200 °C




[TI: E. Ogawa and J. McPherson, IEEE-IRPS, 312(2003)

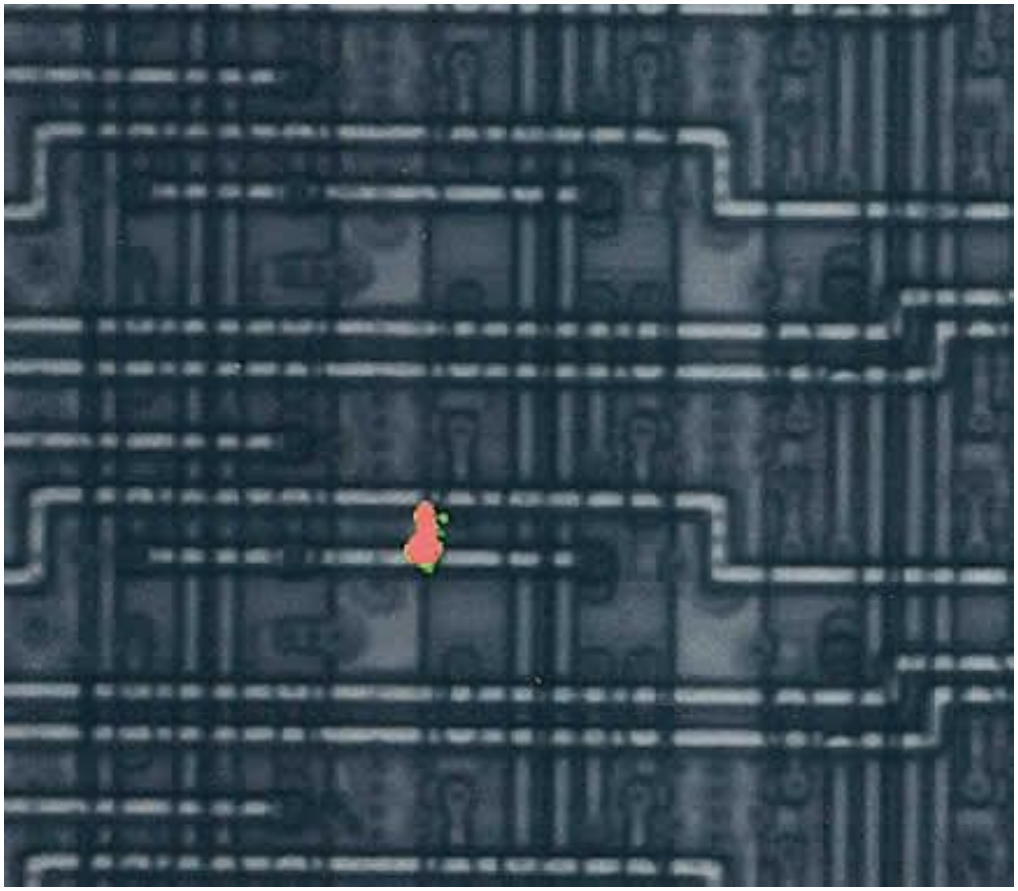
Sources: Ki-Don Lee, et al., "VIA PROCESSING EFFECTS ON ELECTROMIGRATION IN 65 NM TECHNOLOGY", 44th Annual IRPS, 2006.
IRPS Tutorials 2011.

# Time Dependent Dielectric Breakdown

- Failure mechanism in MOSFETs, when the gate oxide breaks down as a result of long-time application of relatively low electric field (as opposite to immediate breakdown, which is caused by strong electric field).

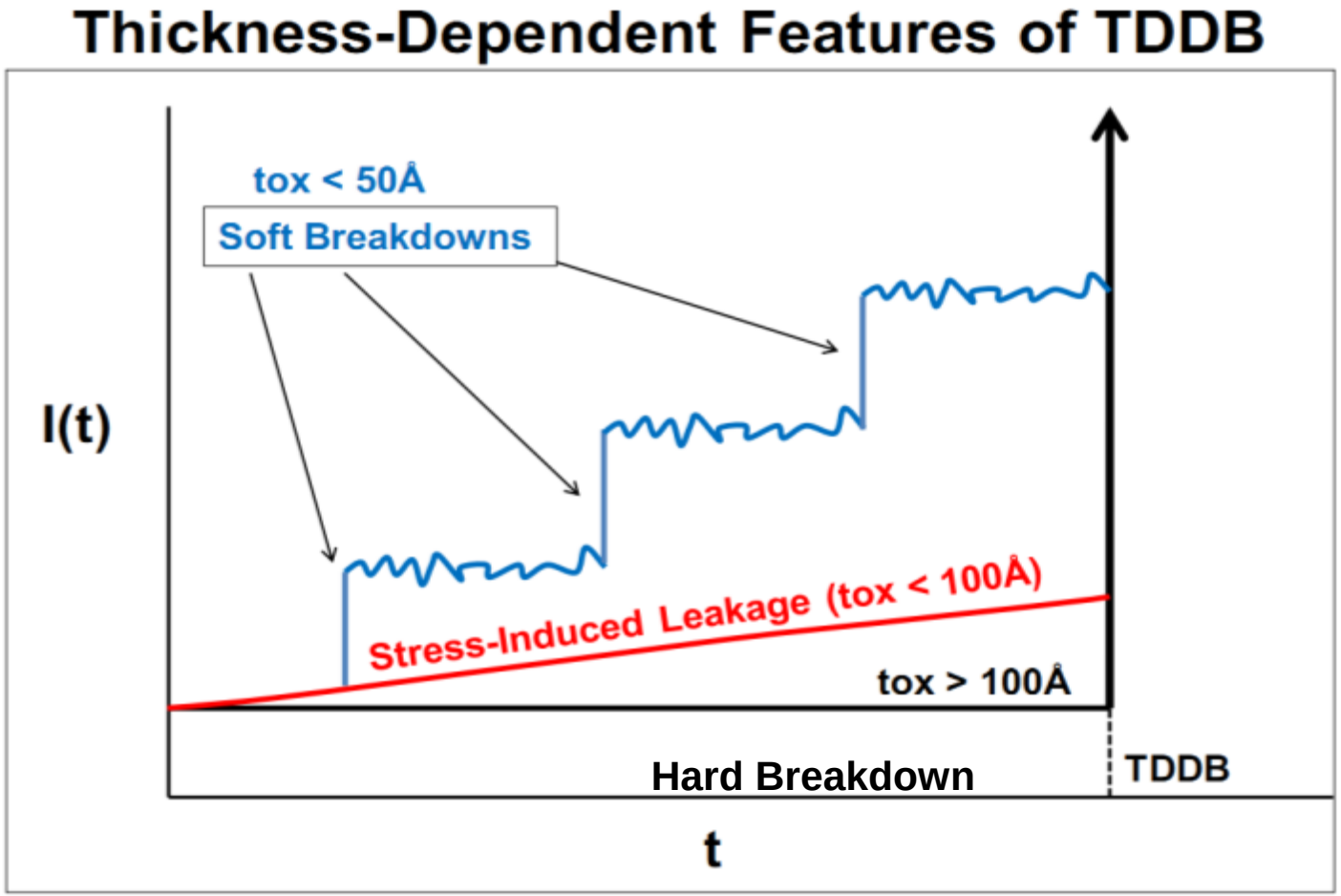
- The breakdown is caused by formation of a conducting path through the gate oxide to substrate due to electron tunnelling current, when MOSFETs are operated close to or beyond their specified operating voltages.

# Time-Dependent Dielectric Breakdown (TDDB)



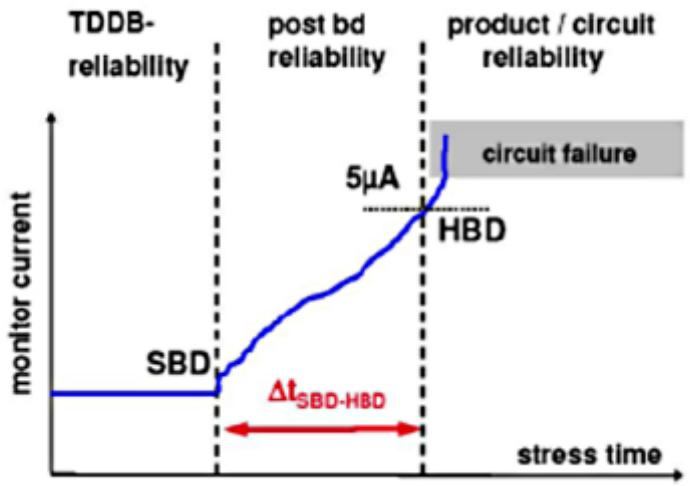
Short caused by TDDB is seen in this thermal camera image.

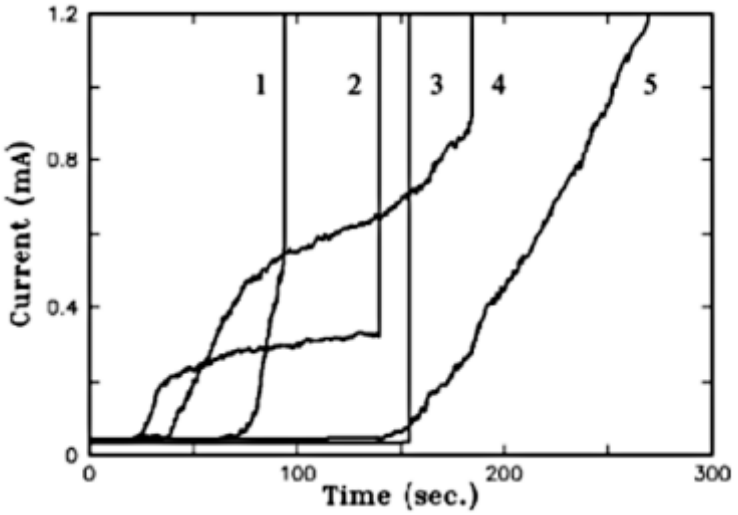
# TDDB (Types of Breakdown)

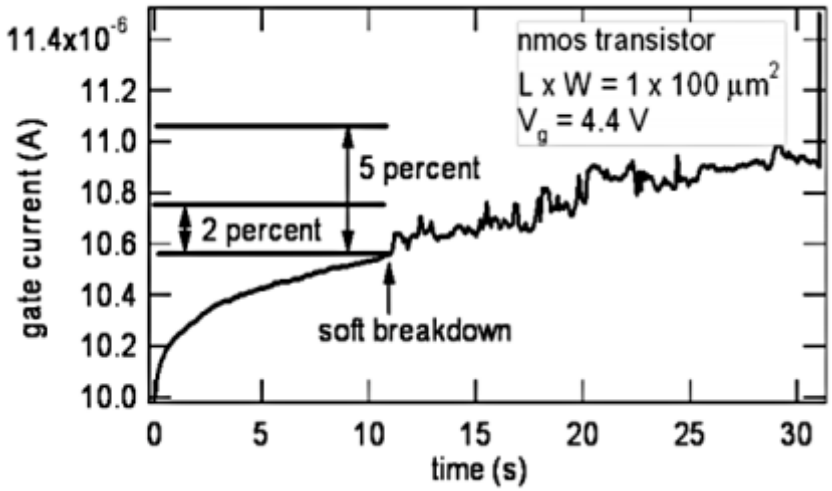



Source: IRPS 2011 Tutorials

# TDDB (Types of Breakdown)



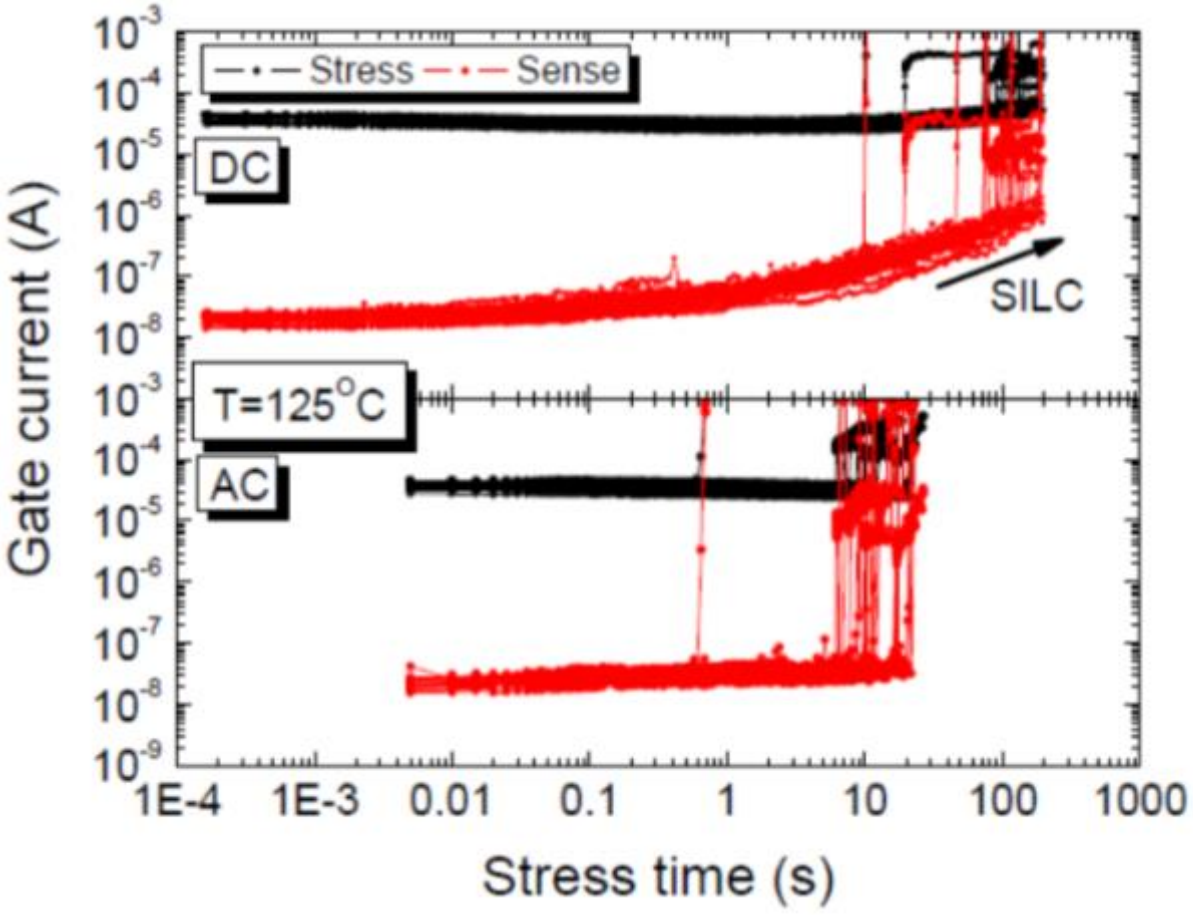




Criteria between TDDB types are not well-defined.

Source: IRPS 2011 Tutorials

# TDDB (DC stress vs. AC stress)




DC and AC stresses may cause completely different results => Need to characterize both stress modes.

Source: IRPS 2011 Tutorials

# Hot Carrier Injection (HCI)

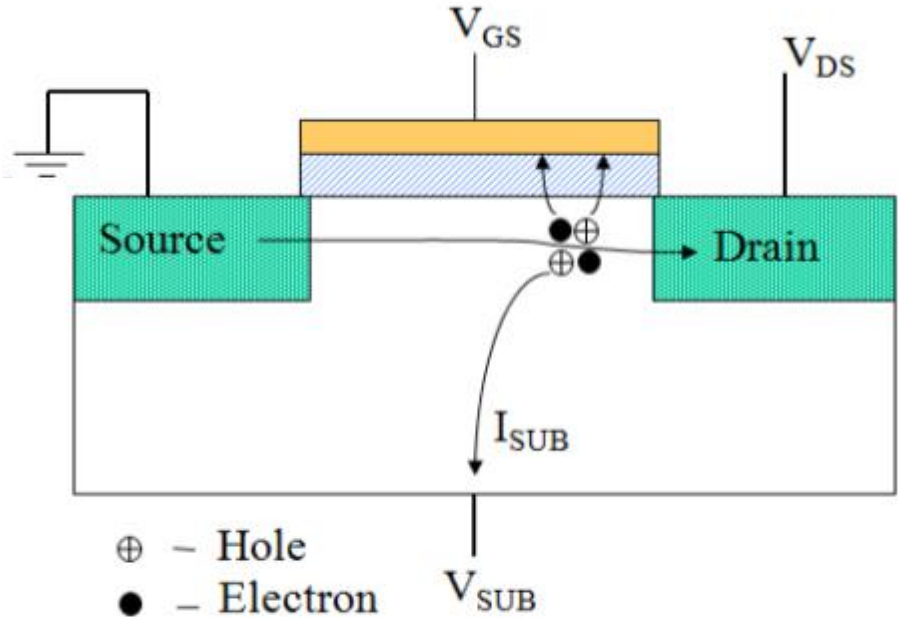
- A phenomenon in where an electron or a hole gains sufficient kinetic energy to overcome a potential barrier necessary to break an interface state.
  - To become “hot” and enter the conduction band of SiO2, an electron must gain a kinetic energy of 3.3 eV. For holes, the valence band offset in this case dictates they must have a kinetic energy of 4.6 eV.
  - The term "hot electron" comes from the effective temperature term used when modelling carrier density and does not refer to the actual temperature of anything.
  - High temperatures caused by the effect are unrelated to the phrase "hot electron effect".
- Carrier is injected from channel into gate dielectric
- Effects include heating of the device and increased leakage current.
  - Heating is caused by “hot” electrons giving off their excess energy as phonons.

# Hot Carrier Degradation

## Hot Carrier – Physics of Failure

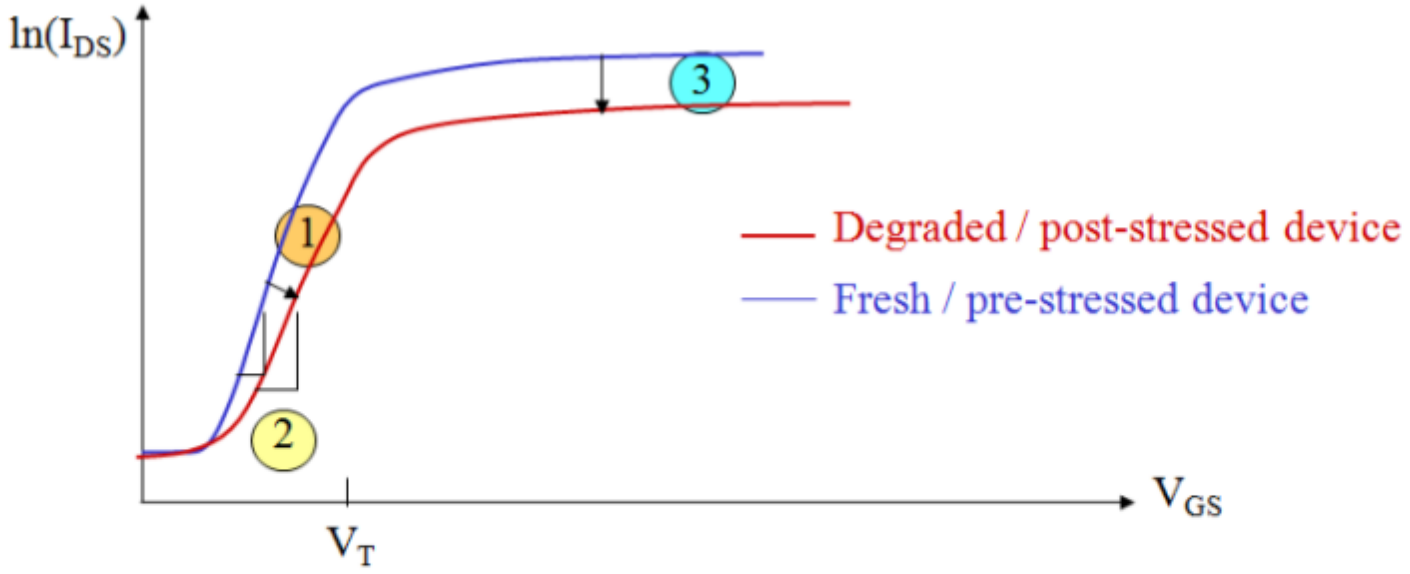
**Drain Avalanche Hot-Carrier Injection**

- Impact ionization
  - Energetic electrons excite other $e^-$'s from VB to CB
  - Holes created at VB
- Holes are attracted toward:
  - Substrate contact
  - Gate oxide (low $V_{GS}$)
- Electrons go toward:
  - Drain contact
  - Gate oxide (mid and high $V_{GS}$)



# Hot Carrier Degradation

## Hot-carrier induced effects




1. Parallel shift of I-V curve due to oxide trapped charge $N_{ot}$ => Increase in $V_T$
2. Stretch-out of I-V curve due to interface states $N_{it}$ => Decrease in 's'
3. Decrease in transconductance due to mobility degradation => Decrease in $I_{Dsat}$

# Hot Carrier Degradation

**Fabs do not give enough reliability test data to designers and reliability engineers**

| Qual Items | DUT | Structures | Sample size | Stress Conditions | Failure Criteria | Specifications | Result |
|---|---|---|---|---|---|---|---|
| Gate oxide VBD | 1.2V Core | Area = 5e2 ~ 2.4e3 um$^2$ | >=3 wafer/lot; 3 lots; 25,560 | Voltage ramp 3.3V/s (inversion mode) | Ig leak > 40uA @ 1V | Do <= 5/cm$^2$ @ VBD <= 1.2V<br>Do <= 1/cm$^2$ @ 1.2V < VBD < 2.9V | Pass |
| | 2.5V I/O | Area = 4.8e3 ~ 1e6 um$^2$ | | Voltage ramp 6.27V/s (accumulation mode) | Ig leak > 15uA @ 1.5V | Do <= 5/cm$^2$ @ VBD <= 2.5V<br>Do <= 1/cm$^2$ @ 2.5V < VBD < 5.0V | Pass |
| | 2.5V I/O over drive | | | Voltage ramp 6.27V/s (accumulation mode) | Ig leak > 15uA @ 1.5V | Do <= 5/cm$^2$ @ VBD <= 3.3V<br>Do <= 1/cm$^2$ @ 3.3V < VBD < 7.2V | Pass |
| Gate oxide TDDB | 1.2V Core | Area ~ 1e7 um$^2$ (W/L=1/0.06) | >= 50/stress/lot; 3 lots | 3-5 stress voltage @ 125C & field ~ 8-12MV/cm | 1st soft breakdown | TTF @0.1% cum failure rate > 10yr for 0.1cm$^2$ @ 125C & 1.2V+10% | Pass |
| | 2.5V I/O | Area ~1e6 um$^2$ (W/L=4/4.8 x 2000) | | 3-5 stress voltage @ 125C & field ~ 8-12MV/cm | Hard breakdown | TTF @0.1% cum failure rate > 10yr for 0.01cm$^2$ @ 125C & 2.5V+10% | Pass |
| | 2.5V I/O over drive | | | 3-5 stress voltage @ 125C & field ~ 8-12MV/cm | Hard breakdown | TTF @0.1% cum failure rate > 10yr for 0.01cm$^2$ @ 125C & 3.3V+10% | Pass |
| PID | 1.2V Core | W/L=5/0.2 | >= 4 wafer/lot; 3 lots | Ig @Vg=1.4Vcc inversion | Ig tailing | Ig tailing < 5% | Pass |
| | 2.5V I/O | W/L=2.63/0.38 | | Ig @Vg=1.8Vcc (2.6Vcc) for NMOS (PMOS) | | | |
| HCI | 1.2V Core | W/L=1/0.06 | 24/pattern/lot; 3 lots | 1.2V (Vds=Vgs=1.7V, 1.8V, 1.9V, 2.0V) TTF vs 1/Vds | Idsat change > [illegible]% | DC lifetime > 0.2 yr | Pass |
| | 2.5V I/O | W/L=10/0.28 | 15/pattern/lot; 3 lots | 2.5V (Vds=3.3V, 3.5V, 3.7V, Vgs@Isub(max)) TTF vs Isub$^m$ | | AC lifetime > 10 yr | Pass |
| | 2.5V I/O over drive | W/L=10/0.5 (N), 10/0.4 (P) | | 2.5V (Vds=4.1V, 4.3V, 4.5V, Vgs@Isub(max)) TTF vs Isub$^m$ | | 0.1% cum failure @25C, Vc[illegible]0% (Core P @125C) | Pass |
| NBTI | 1.2V Core | W/L=1/0.06 | >= 20/lot; 3 lots | Vg: 6-9 MV/cm @ 125C; Vs=Vd=Vb=grounded | Idsat degrade > 10% | TTF 0.1% cum failure @125C, Vcc+10% >5 yr | Pass |
| | 2.5V I/O | W/L=10/0.28 | | | | | |
| | 2.5V I/O over drive | W/L=10/0.4 | | | | | |
| EM | M1 + contact | W/S=0.09/0.09 (1800 A) | > 20/pattern/lot; 3 lots | Jstess=1-5MA/cm$^2$ @ 300C | dR >10% Ro | TTF 0.1% cum failure @110C > 100k hr | Pass |
| | Mx + Vx | W/S=0.10/0.10 (2200 A) | | | | | |
| | My + Vy | W/S=0.20/0.20 (5000 A) | | Jstess=1-5MA/cm$^2$ @ 350C | | | |
| | Al-Cu RDL | W/S=3/2 (14.5K A) | | Jstess=1-5MA/cm$^2$ @ 250C | | | |
| SM | Vias chain | metal-via overlap from min to 0.7 | >130/lot; 3 lots | 500 hr bake @175C | dR >10% Ro | No failure allowed | Pass |
| IMD Low-K TDDB | M1, V1, M2 combs | M1 & M2 W/S=Min/Min<br>V1 W/S=0.10/0.13 | >30 /pattern/lot; 3 lots | 2.5-4.0 MA/cm @ 125C | I(TBD) = 100 x I(T=0) | TTF 0.1% cum failure @125C & 3.6V > 10 yr | Pass |

DC lifetime for Hot Carrier >**0.2 yr**, AC lifetime >**10 yr** in a 65 nm CMOS process

http://www.siliconbluetech.com/media/downloads/SBT_65LP_Process_Qual_v0.1.pdf

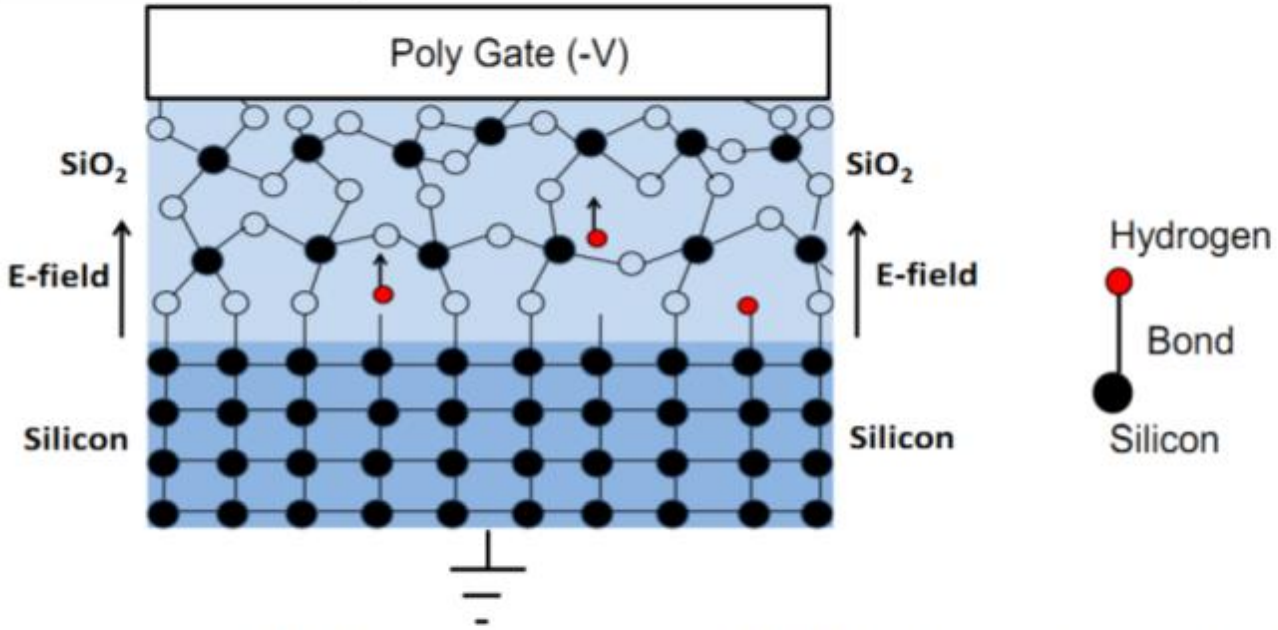
# NBTI & PBTI

- Negative bias temperature instability (NBTI) is a key reliability issue for PMOS.
  - PMOS operate almost always with negative gate-to-source voltage
  - The very same mechanism affects also NMOS when biased in the accumulation regime (PBTI)
- NBTI manifests as
  - an increase in threshold voltage
  - A decrease in drain current and transconductance.
  - The degradation has  logarithmic dependence on time.
- Two kinds of trap contribute to NBTI:
  - Interface traps
    - → cannot be recovered over a reasonable time of operation - permanent traps
    - → similar to the ones resulting from HCI
    - → In case of NBTI, the electric field breaks Si-H bonds located at the SiO2 interface. H is released and migrates in the substrate. The remaining dangling Si- bond contribute to Vth degradation.
  - Pre-existing traps located in the bulk of the dielectric (and supposedly nitrogen related), are filled with holes coming from the PMOS channel. Those traps can be emptied when the stress voltage is removed. This Vth degradation can be recovered over time. (Annealing effect)

# NBTI and PBTI

## Negative-Bias Temperature Instability (NBTI)

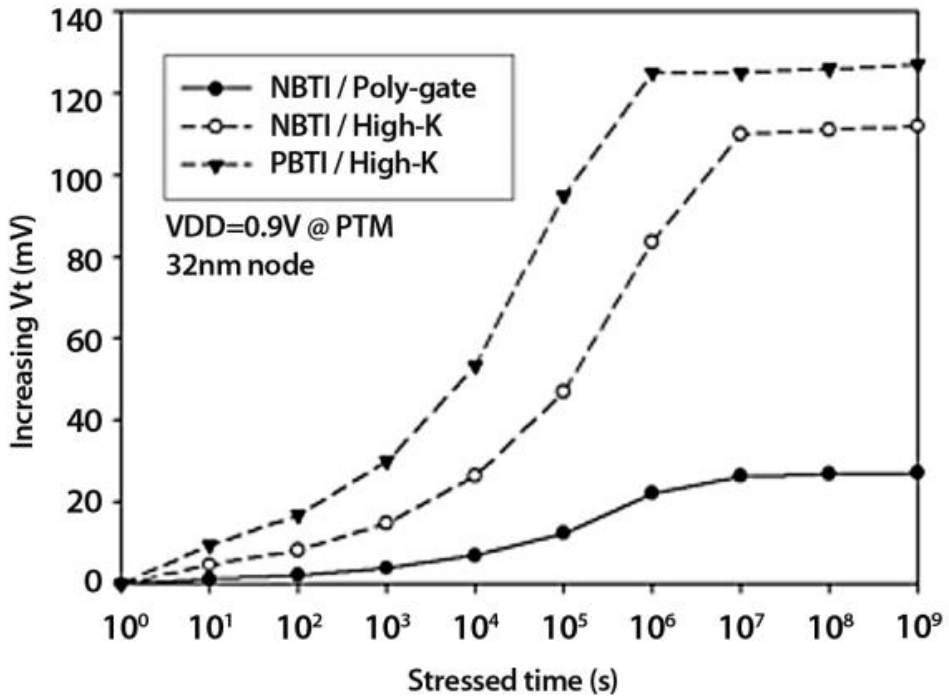
**P-MOSFET ISSUE**

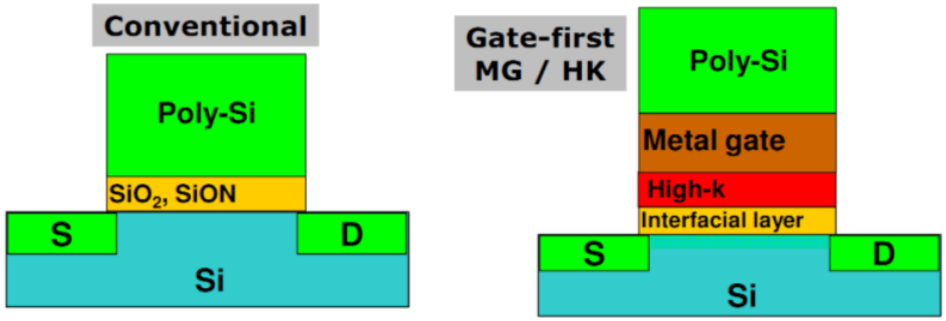



During normal P-MOS operation, interfacial Si-H bonds can become broken. Negative gate voltage serves to produce more holes at the Si surface. Hole absorption by the Si-H bond can serve to free the hydrogen which can then can diffuse away from the Si-O interface resulting in interface-state generation and a $V_{th}$ shift. Si-H bonds are more easily broken at higher temperatures.

Source: IRPS 2011 Tutorials

# NBTI and PBTI

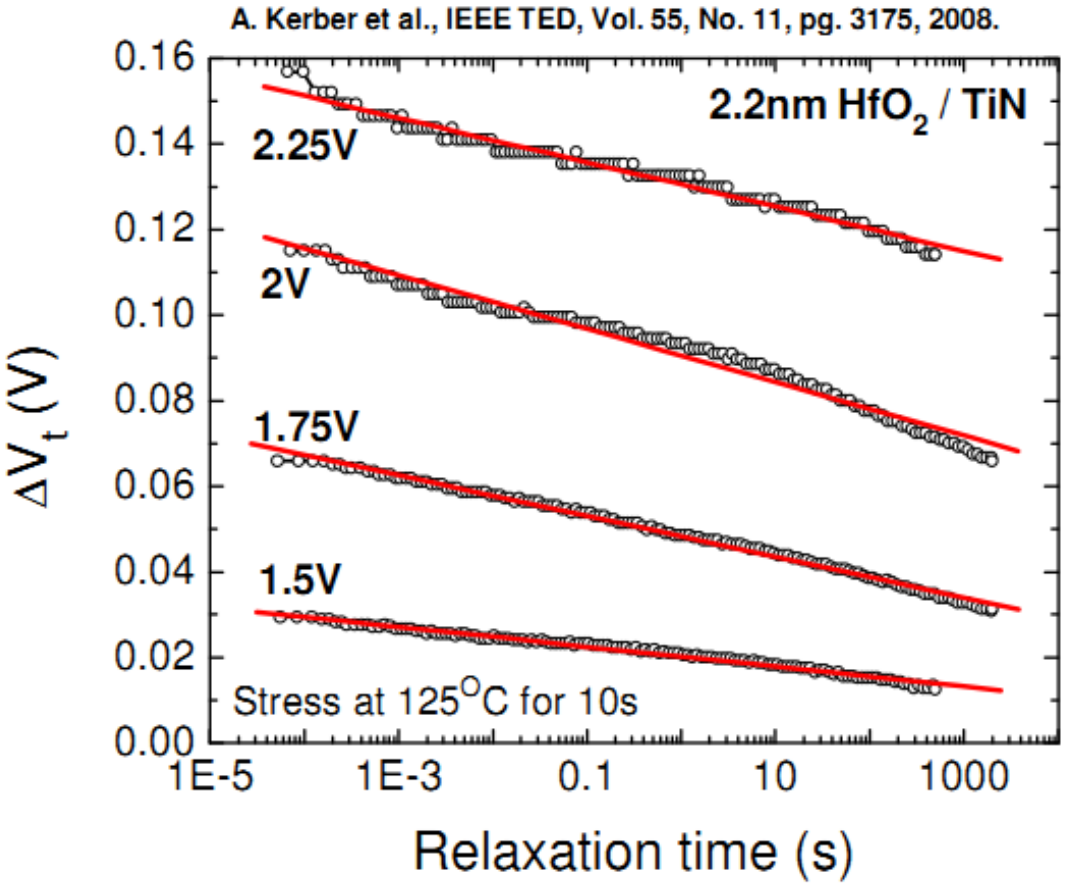



NBTI/PBTI-induced $V_T$ drifts vs. stressed time for 32 nm poly-gate
and high-k metal-gate devices.

Source: Shyh-Chyi Yang, et. Al TIMING CONTROL DEGRADATION AND NBTI/PBTI TOLERANT DESIGN FOR WRITE-REPLICA CIRCUIT IN NANOSCALE CMOS SRAM, VLSI-DAT '09.

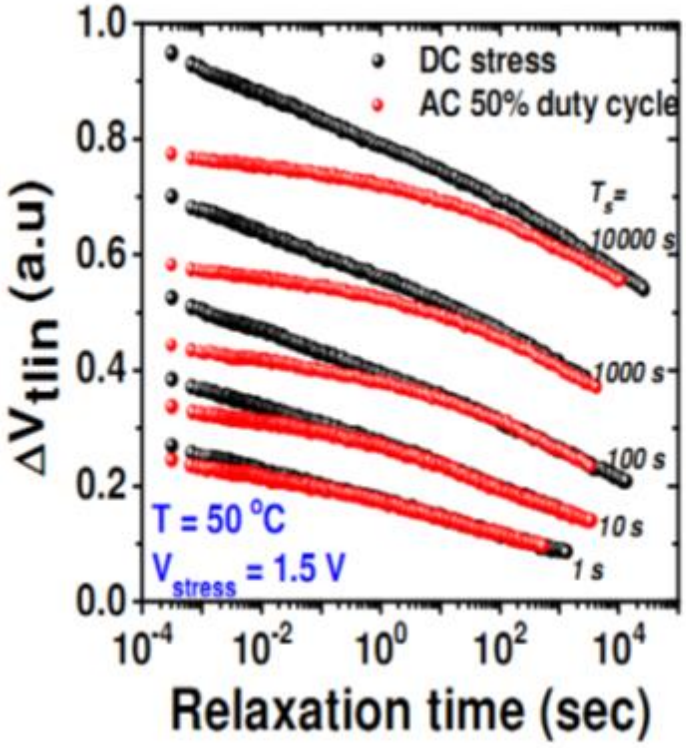
# NBTI and PBTI (Relaxation)

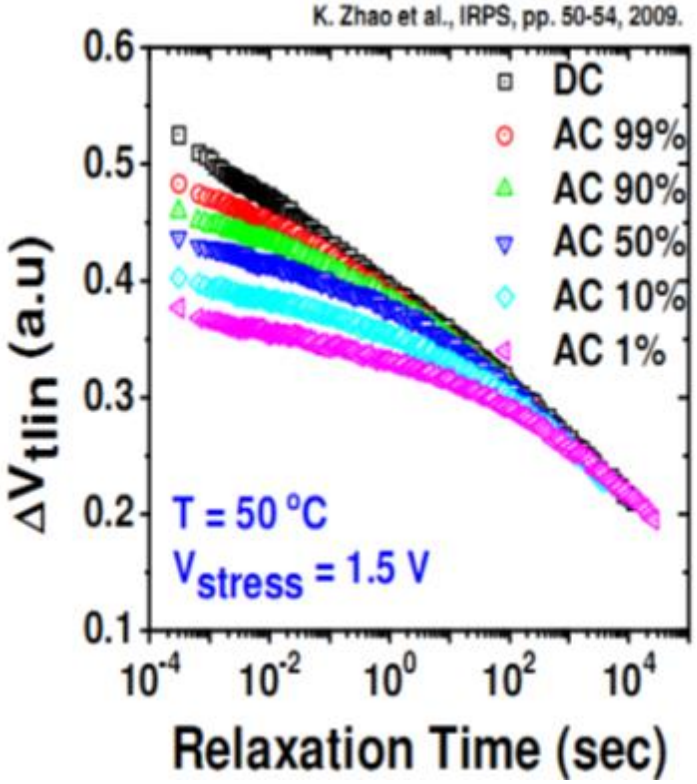



Example of PBTI Relaxation => Fast measurement is required.

# NBTI and PBTI (DC vs. AC stress)

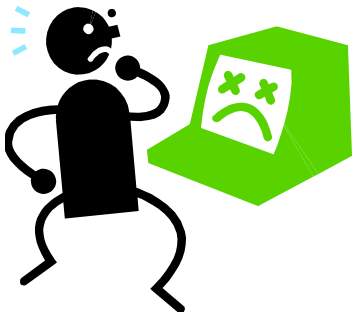
## Impact of Stress Mode on PBTI Relaxation




Source: IRPS 2011 MG HK Tutorial

# Our Customers' Problems



Customer 1:
"Foundries do not give us enough reliability test / process data"

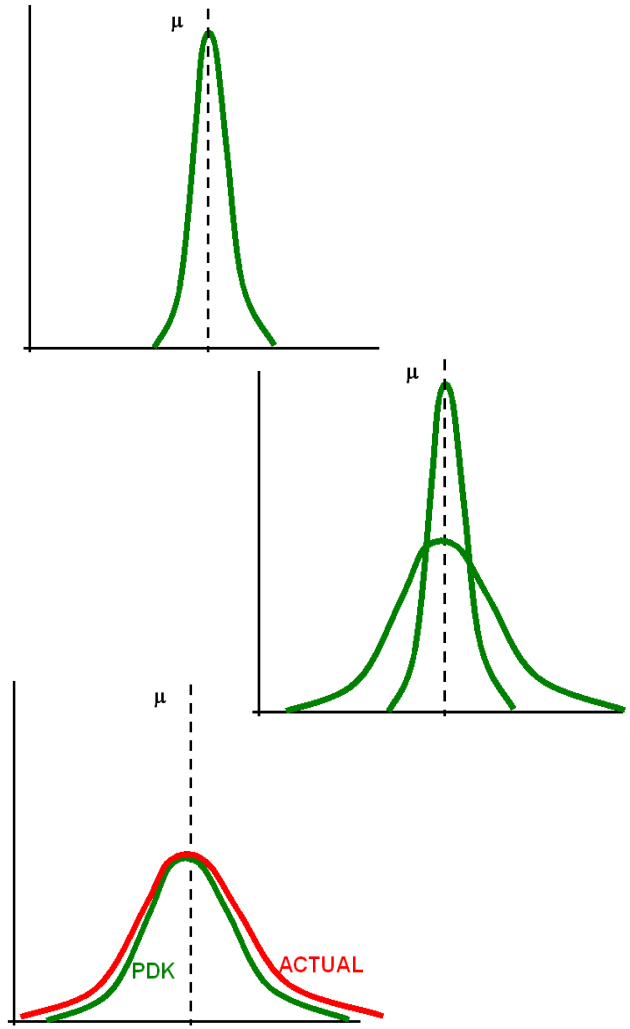
Customer 2:
"We can test only three DUTs in parallel and the test lasts a full month"

# Overview of the Existing Problem

- Small-geometry fabrication processes are very complex
- Reliability concerns for demanding applications include:
  - Bias Temperature Instabilities
  - Dielectric Breakdown
  - Hot Carrier Effects
  - Electro- / Stress Migration
  - Process Mismatch Effects
  - Lot-to-lot Variation
- For space and radiation-sensitive applications there are also:
  - Single-event radiation effects
  - Total dose radiation effects
- Current techniques are not:
  - Comprehensive enough
  - Accurate enough
  - Fast enough

# Mitigation – Process Data

- Semiconductor processing always yield a distribution of parameter values
- Minimum geometries have larger fluctuations
- Smaller feature size & lower voltages increase the impact of variation of transistor properties on chip performance and yield
- Foundry-supplied Process Design Kit (PDK) may not give sufficiently accurate data for critical design parameters



# PDK versus Die Data

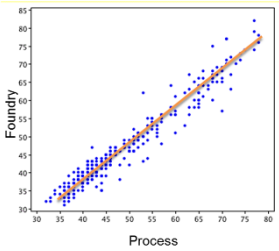
- Process Design Kit (PDK) may not be accurate for particular batch/wafer/die/package
- PDK may not have data for particular application (e.g., temperature)
- PDK may not be representative of particular biasing schemes (e.g., MOSFET matching differs for strong inversion and sub-threshold)
- Data is not placement-specific (directional/wafer angle)
- PDK may not give values to insert into random parameter fluctuation simulations

# Characterization Systems Should…

Deliver lots of data

- Quickly
- Accurately & repeatable
- For different devices
- For different operating conditions

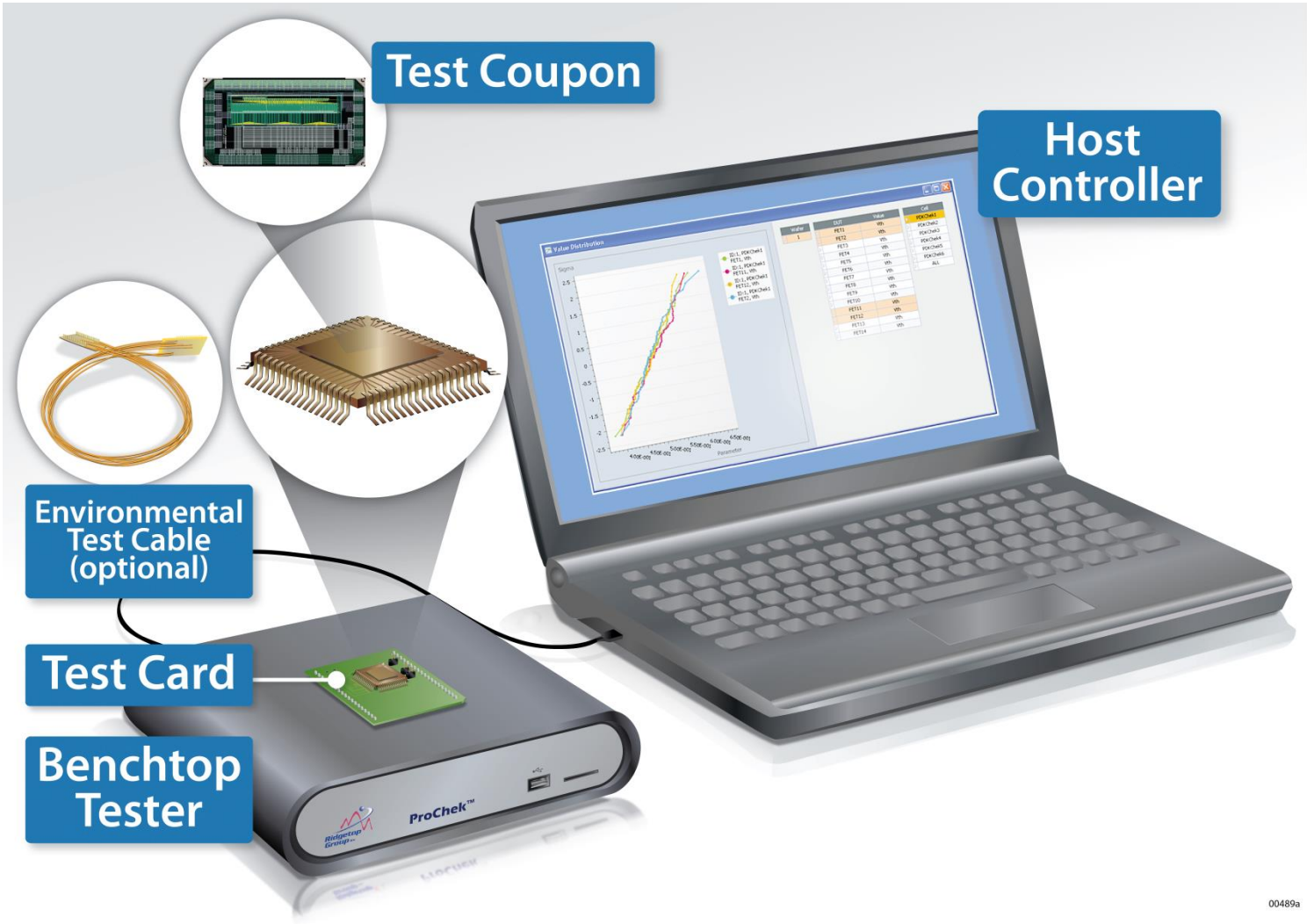
Be inexpensive to own and operate


Allow for direct correlation across foundries and processes

Be easy to use

# Solution: ProChek *(Process Checker)*



# What is ProChek?

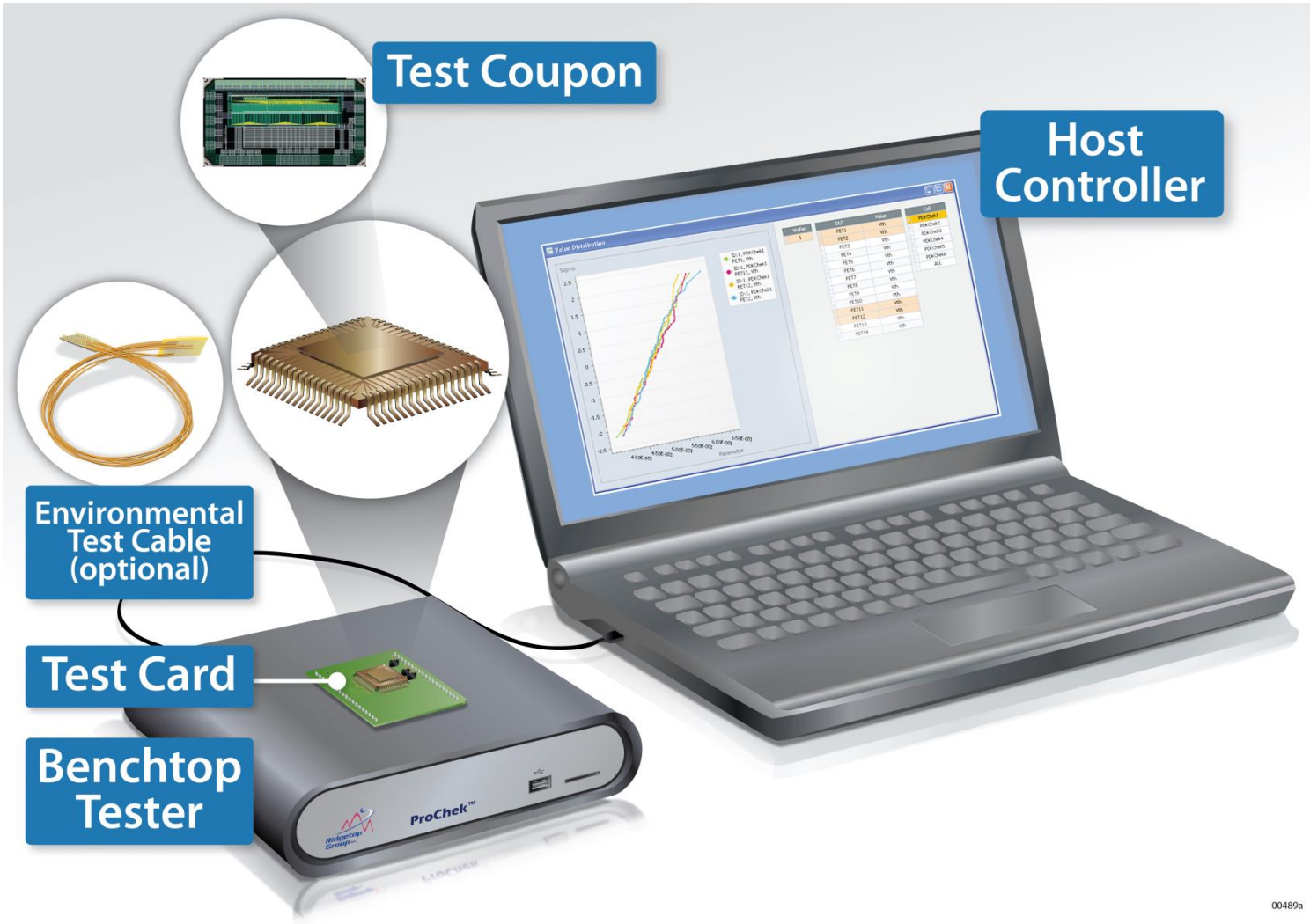
An innovative low-cost technique to rapidly


characterize intrinsic process reliability and monitor process quality

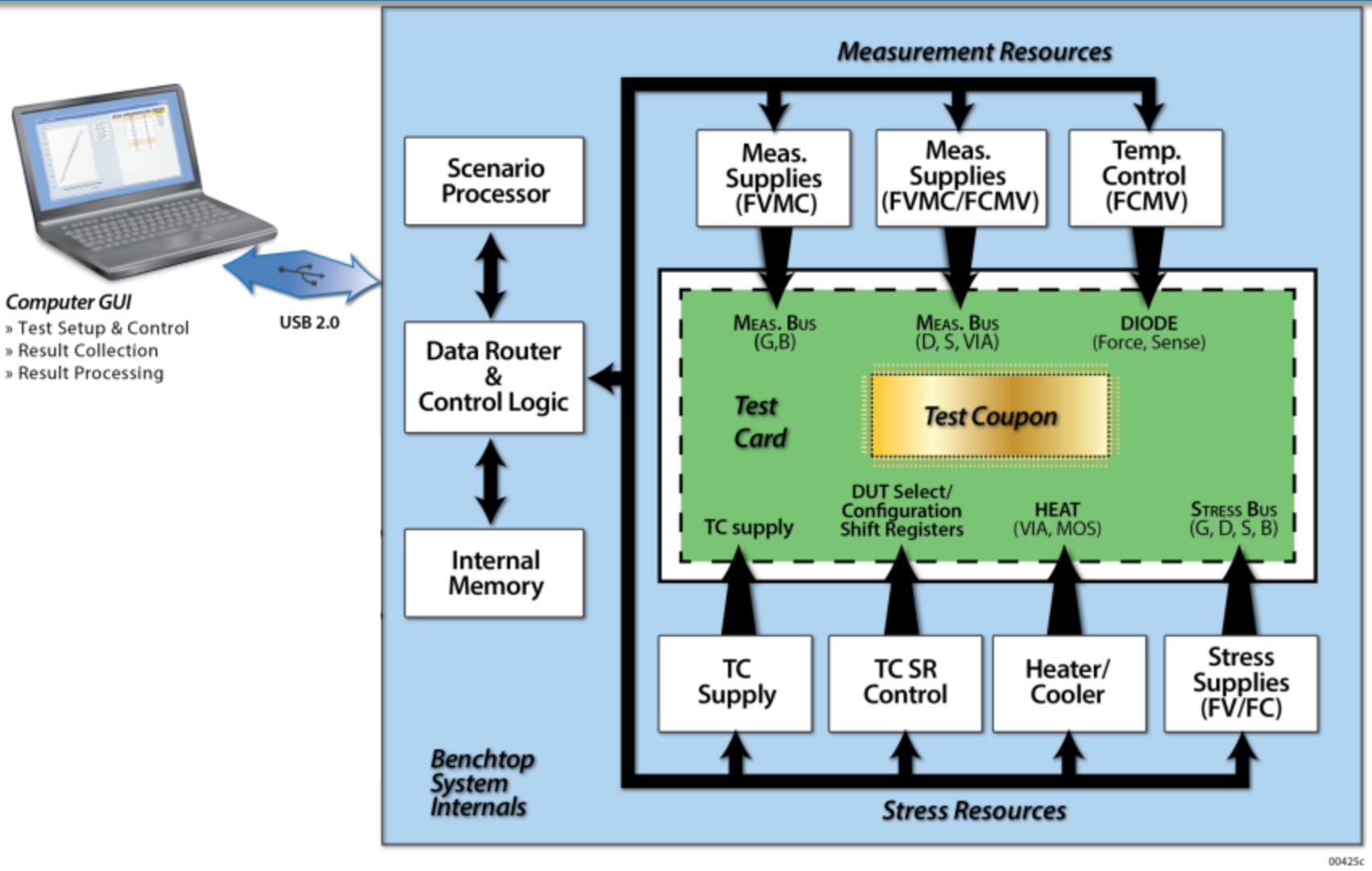
## ProChek…

- Is a flexible & dedicated semiconductor qualification and reliability characterization system.
- Is based on a cost-effective bench-top instrument.
- Can work with a dedicated test chip or with existing test structures.
- Accelerates testing of semiconductor devices in volume.

# ProChek Solution Components



# ProChek Benchtop Tester Architecture



# ProChek Test Coupon

## What

- Combination of test structures, switch matrix and control logic
- Similar test structures are grouped in blocks
- Test structures in a block are stressed concurrently and measured individually

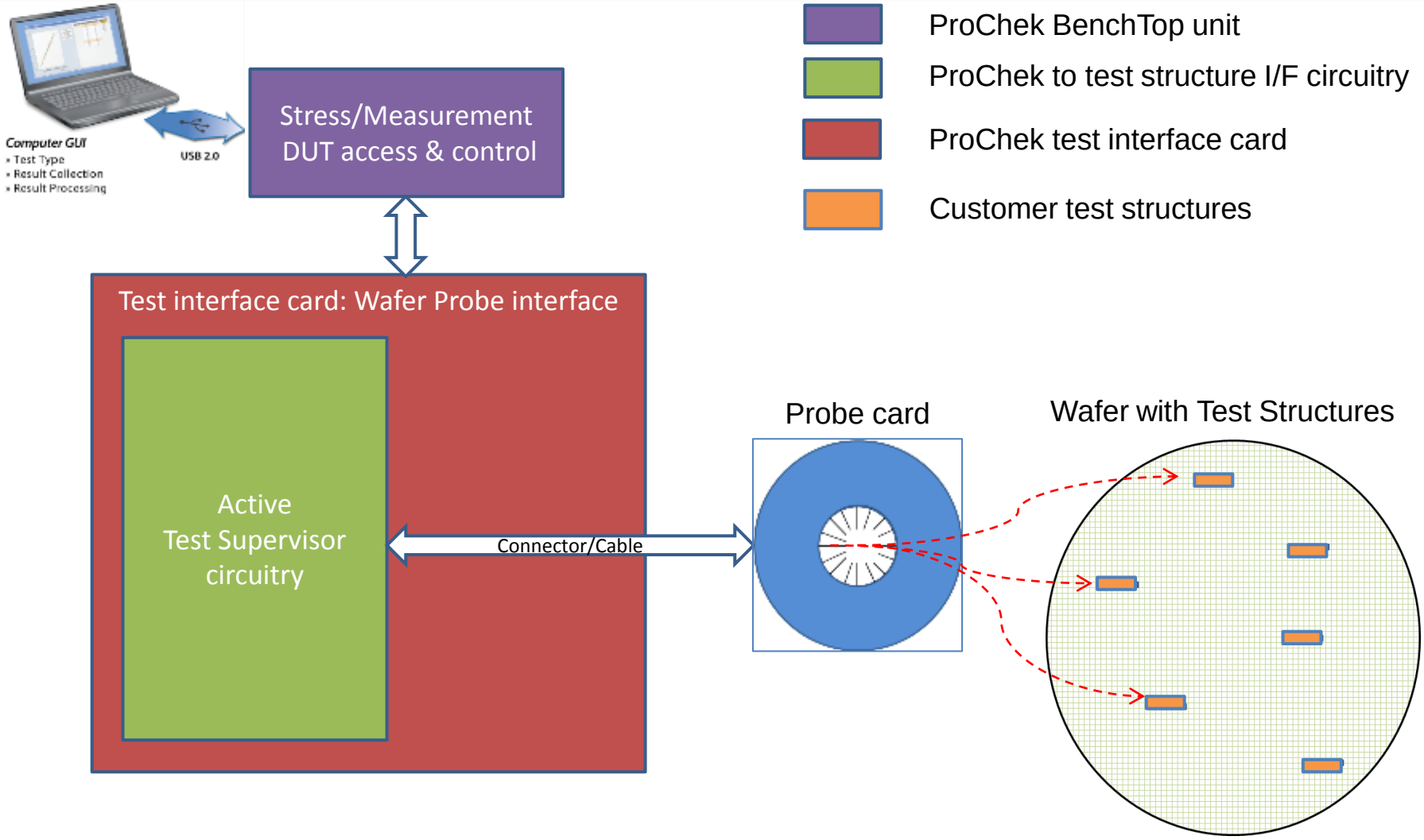
## Existing test structures

- Wafer level or packed structures
- Combined with an active interface board

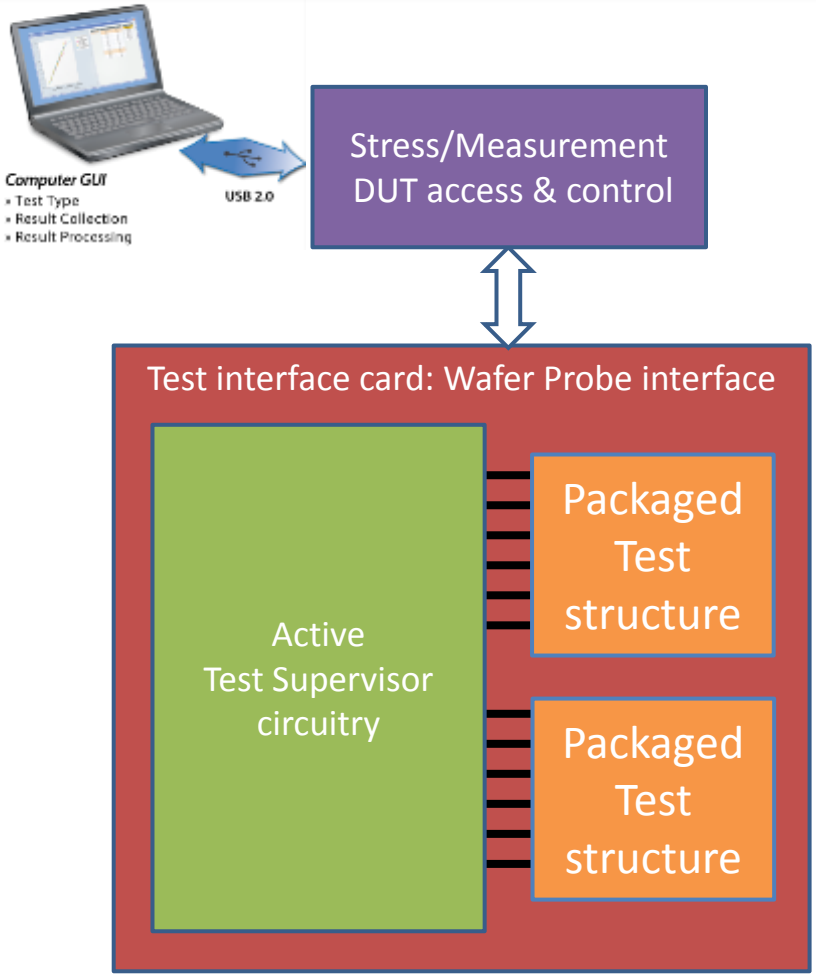
## Dedicated ProChek Test structure

- Integrated Single chip containing test structures, stress features and control circuitry
- Multi-chip solution

# Customized Wafer Probe Interface



# Customized Package Interface




ProChek BenchTop unit

ProChek to test structure I/F circuitry

ProChek test interface card

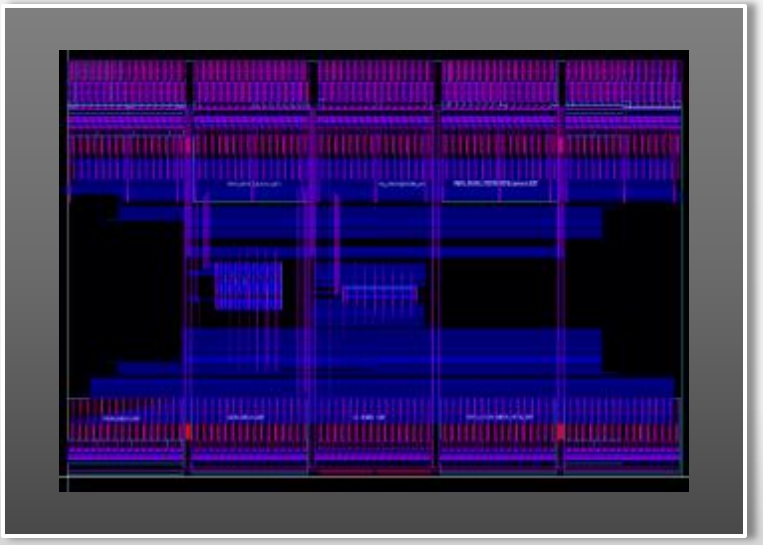
Customer test structures

One (or more)
packaged devices
with
Test Structures

# Types of ProChek Test Coupons

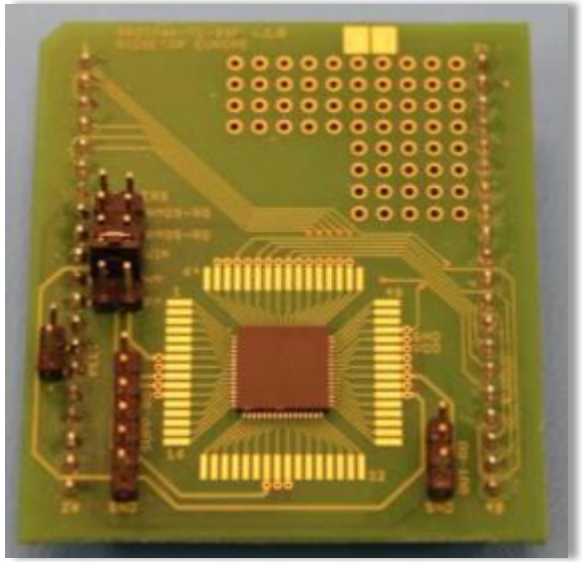
## Integrated Test Coupon

- DUT test structures, control, selection logic, switches, and heaters on a single die.
- Requires both:
  - “Mature”, well defined process, for which there is a stable and well-qualified PDK
  - Process featuring more robust transistors than the DUT test structures

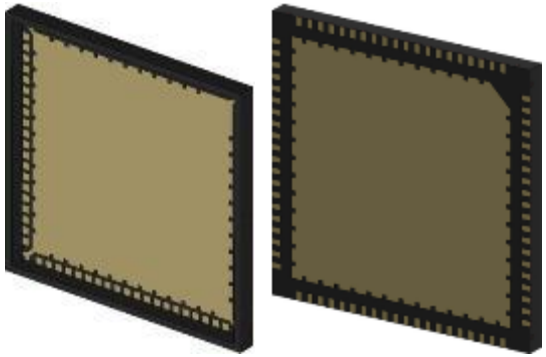


# Integrated ProChek Test Coupon

- The Test Coupon contains the DUTs, heaters, temperature sensors, switches and control structures (the on-chip switching matrix) necessary for performing reliability test with the ProChek Benchtop Tester.
- Coupons are packaged in open cavity Plastic or Ceramic packages.
- Packages must have an exposed thermally conductive bulk (usually copper) to ensure good heat conduction.



Packaged ProChek Test Coupon assembled on ProChek Test Card

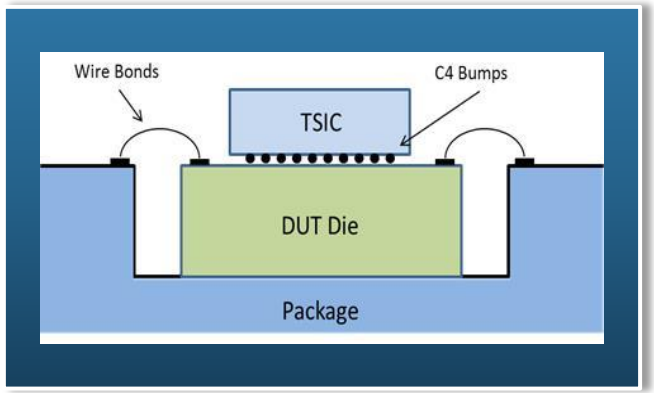


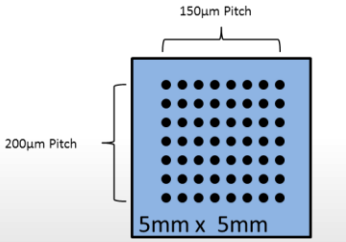
Top and bottom view of package

# Types of ProChek Test Coupons

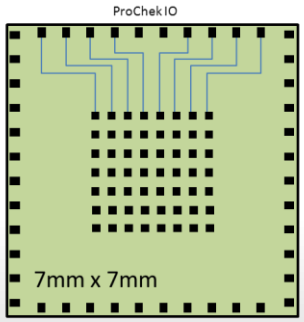
## Multi-chip solution: Test Supervisor IC + DUT IC

- A combined Test Coupon solution consists of a Test Supervisor IC (TSIC) and one or more DUT ICs.
- TSIC:
  - Contains Control and Switching matrix
  - separate die in a mature, higher voltage process.
- DUT IC:
  - DUT structures and heaters
  - separate die using the process of interest.
- The two dies are combined in a single package.



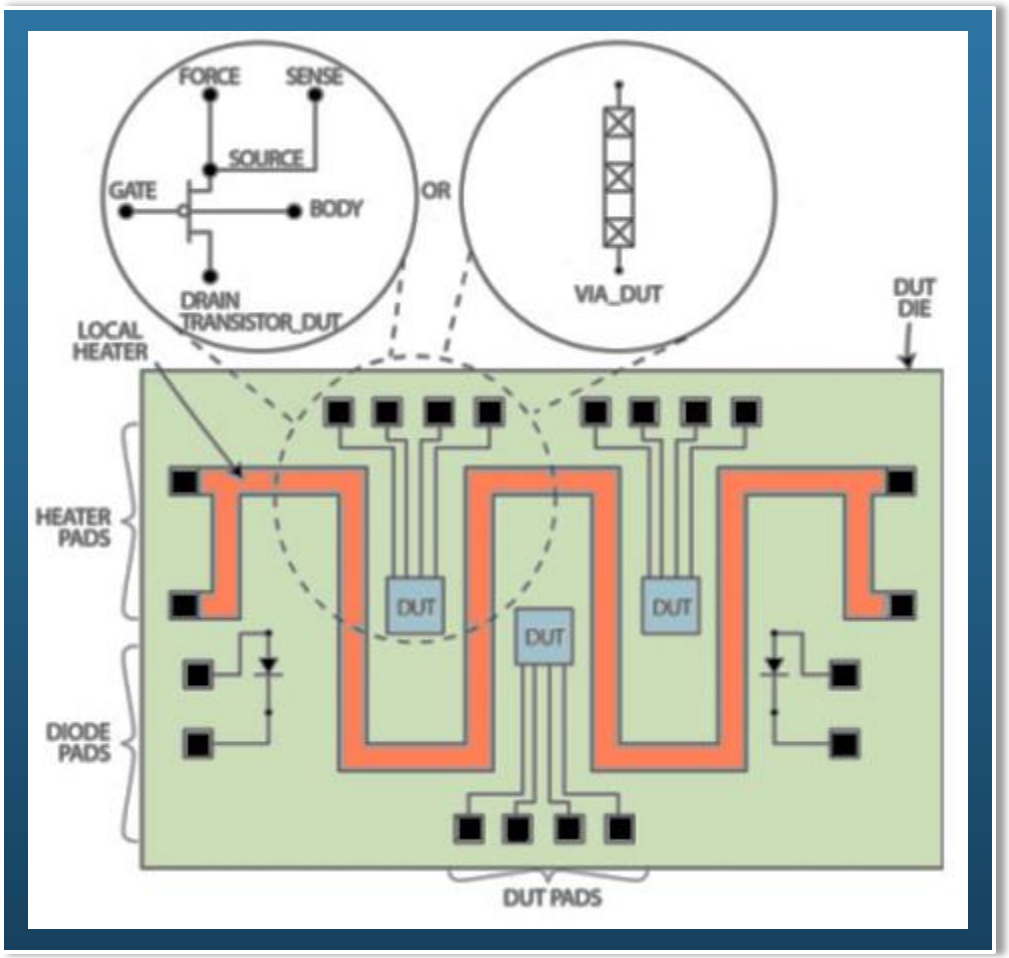




TSIC- High Voltage CMOS




DUT IC – Process of Interest

# ProChek DUT IC

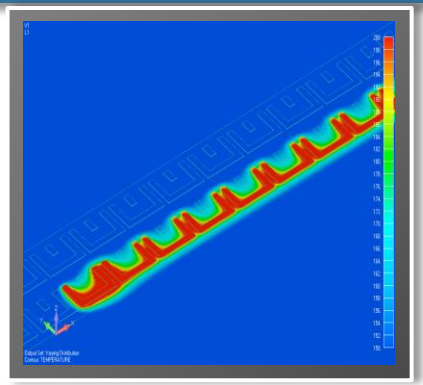



- ProChek DUT IC has an array of DUTs (e.g., transistors, vias) with all terminals padded out.
- Local heaters and temperature measurement diodes are optional.
- One DUT IC typically contains 16 blocks with 8 DUTs of the same type per block
- On-chip local resistive heating elements can be used to significantly increase degradation rate.

# Accelerated Testing

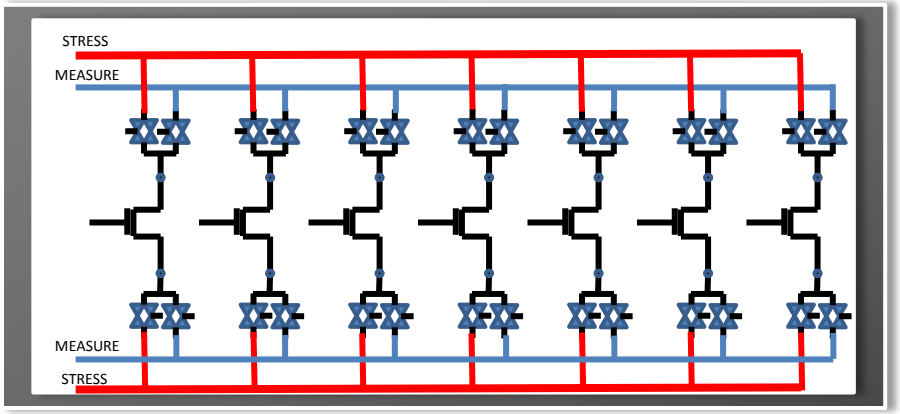
## Combining Thermal and Electrical Overstress

- Peltier device and embedded polysilicon heaters elevate/reduce DUT thermal stress from -30 ˚C to over 300 ˚C
- 4 terminals available to apply electrical stress to each DUT



## Multiple Measurements In Parallel

- High throughput
- Parallel test of 32 – 1024 devices
- Test time reduced from months to hours

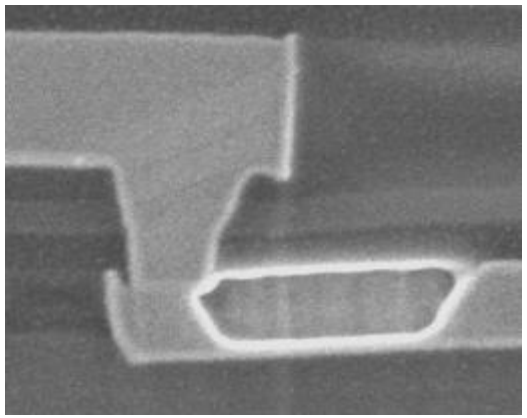



## Parallel Test Systems

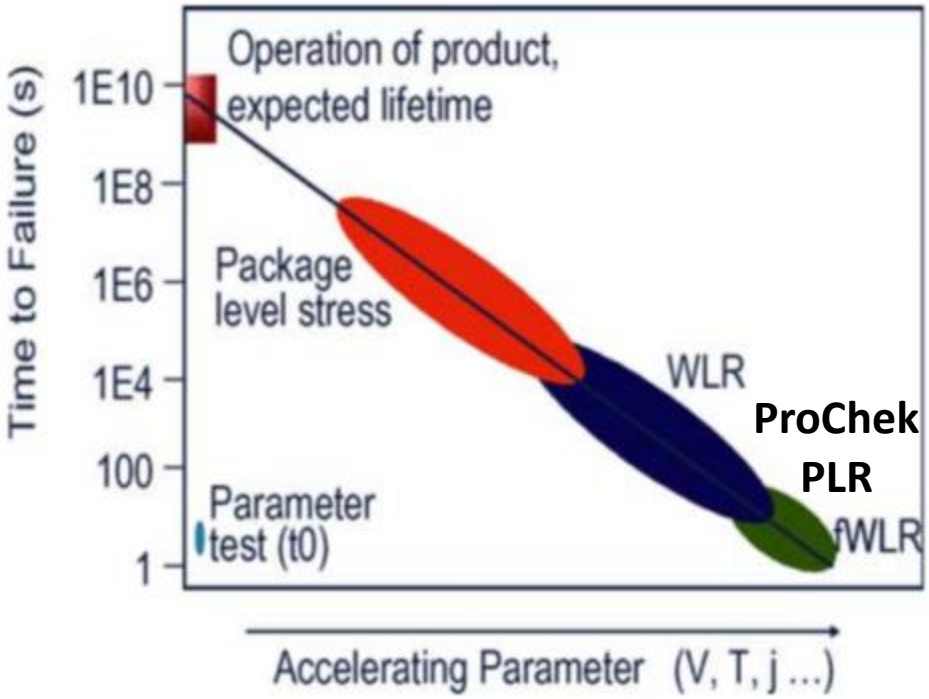
- Up to 8 benchtop instruments may be controlled from a single PC

# Local Heating Structures


Local poly-silicon heaters capable of 325 ˚C will reduce EM, SM and BTI test time and cost

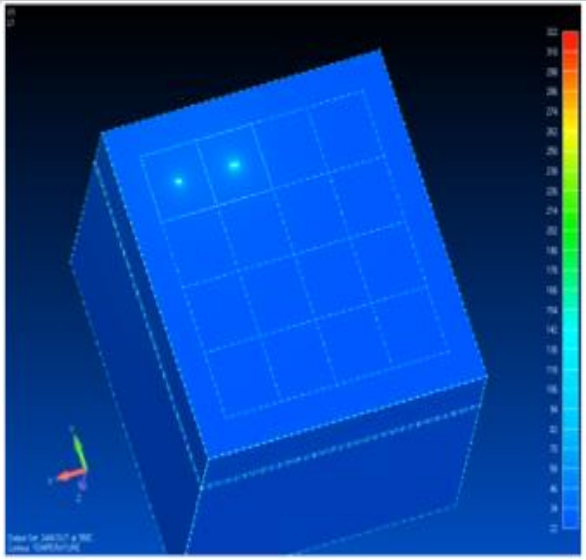


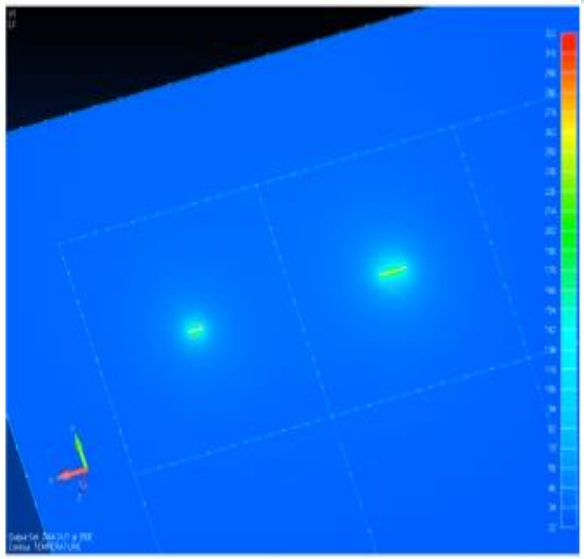
EM-induced void



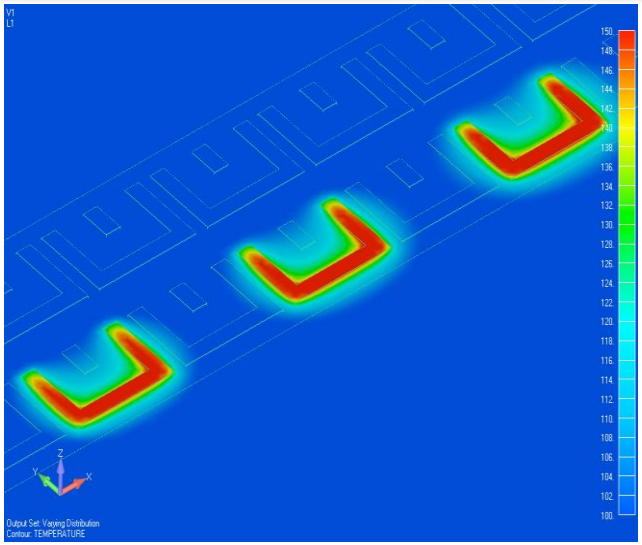

With robust on-chip circuitry and local heaters, ProChek provides as high acceleration factor for package level reliability testing (PLR) on parallel DUTs as currently done for single DUTs in fast Wafer Level Reliability Testing (fWLR).

# Thermal Simulation Results





Two heated DUT arrays are shown on a 2 $mm^2$ (packaged) chip



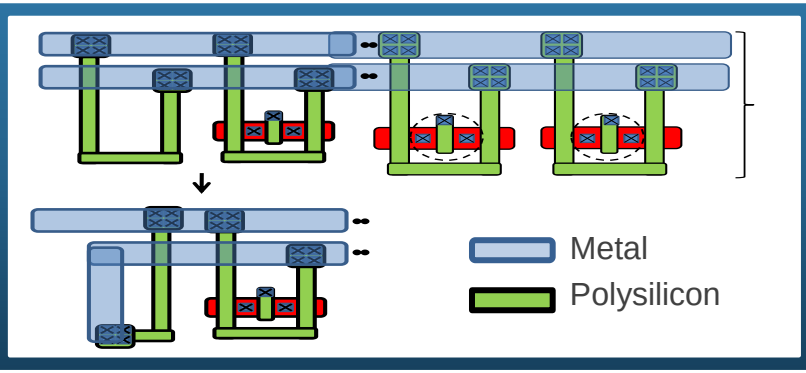
Device-level zoom-in

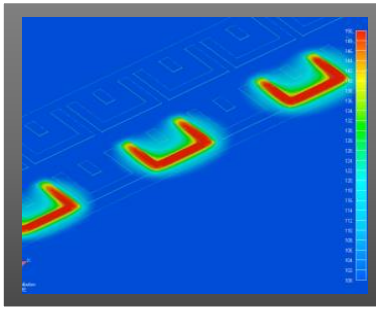
Temperature scale varies from 22 to 322 °C

According to 3D thermal simulations, the localized DUT arrays heat up to 325 °C in 75 milliseconds and consume 16 mW of power per DUT during the test. The temperature drops rapidly on the chip, so the non-stressed structures will not undergo any damage.

# Local Heating Structures

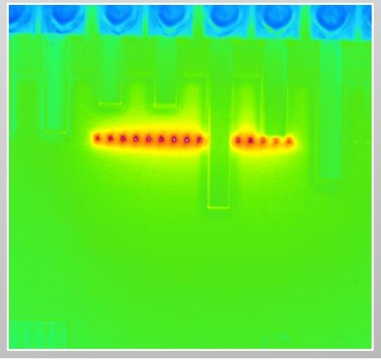
- Polysilicon tracks are used to create a border around each DUT.



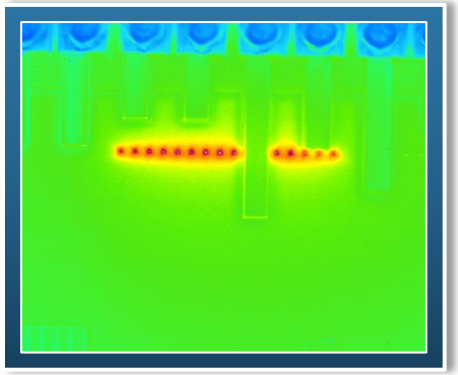
- Localized DUT heaters reach maximum temperature in milliseconds. Non-stressed structures do not undergo any damage.
- Current is forced through these resistive elements to heat the area around the DUTs to over 300 ºC.

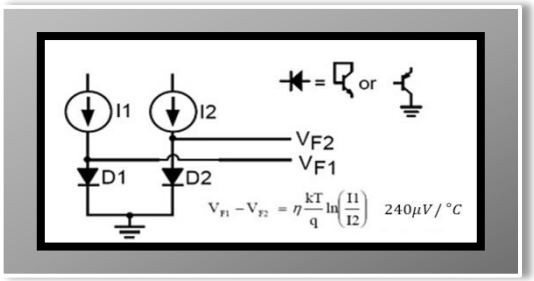
- Infrared camera data from embedded heating test from IBM 8HP test coupon
- Increasing temperatures will reduce EM, SM and BTI test time and cost

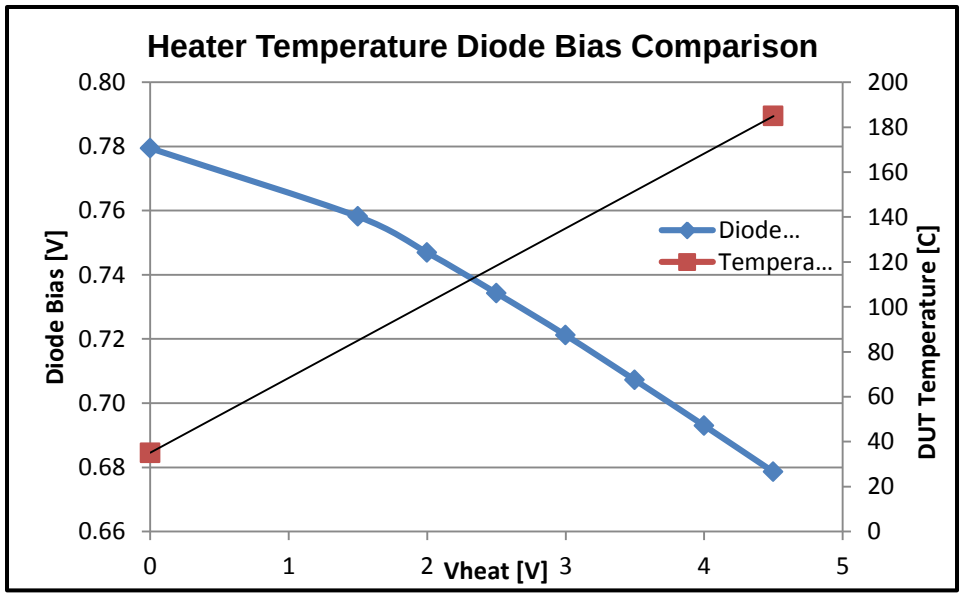


# Heater Calibration

- On-chip diodes are used as sensors to record and regulate DUT temperature.
- Temperature regulation calibration is done by correlation of diode bias voltage with thermal imaging or controlled temperature operation.





# Built-In Test Scenario Descriptions

## Charge to Breakdown – QBD [MOS transistors]

- Gate Current [Ig] is measured against Gate Voltage [Vg] during a destructive ramp of Vg.
- DUTs are tested until oxide breakdown and device destruction.

## Time-Dependent Dielectric Breakdown – TDDB [MOS transistors]

- Ig is measured for a DC bias of Vg.
- DUTs are measured at a programmable frequency, duration, and test temperature.

## Hot Carrier Injection – HCI [MOS transistors]

- Drain-Source Current & Voltage [Ids, Vds], and Ig are measured for a DC Bias or DC sweep of Drain and Gate terminals.
- DUTs are measured at a programmable Vds,Vgs sweep parameters, frequency, duration, and test temperature.

# Built-In Test Scenario Descriptions (cont.)

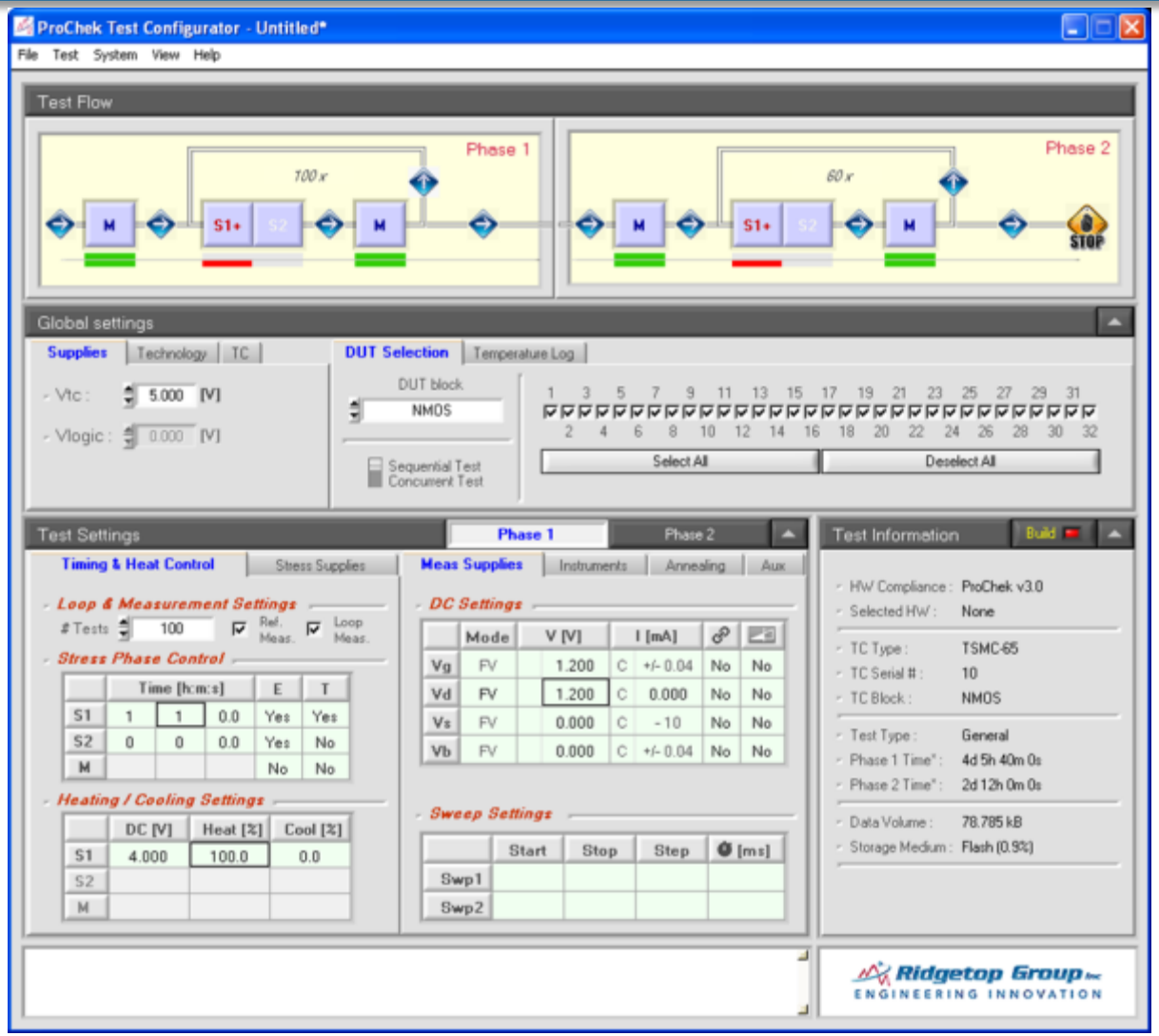
## Bias Temperature Instability – BTI [MOS transistors]

- Ids, Vds, Ig, and Body Current [Ib] are measured for a DC Bias or DC sweep of Drain and Gate terminals.
- Fast annealing observations are available to capture Fast-BTI effects.
- Tests include Stress phase and Relaxation phase to observe stress accumulation and relaxation.
- DUTs are measured at a programmable Vds,Vgs sweep parameters, frequency, duration, and test temperature.

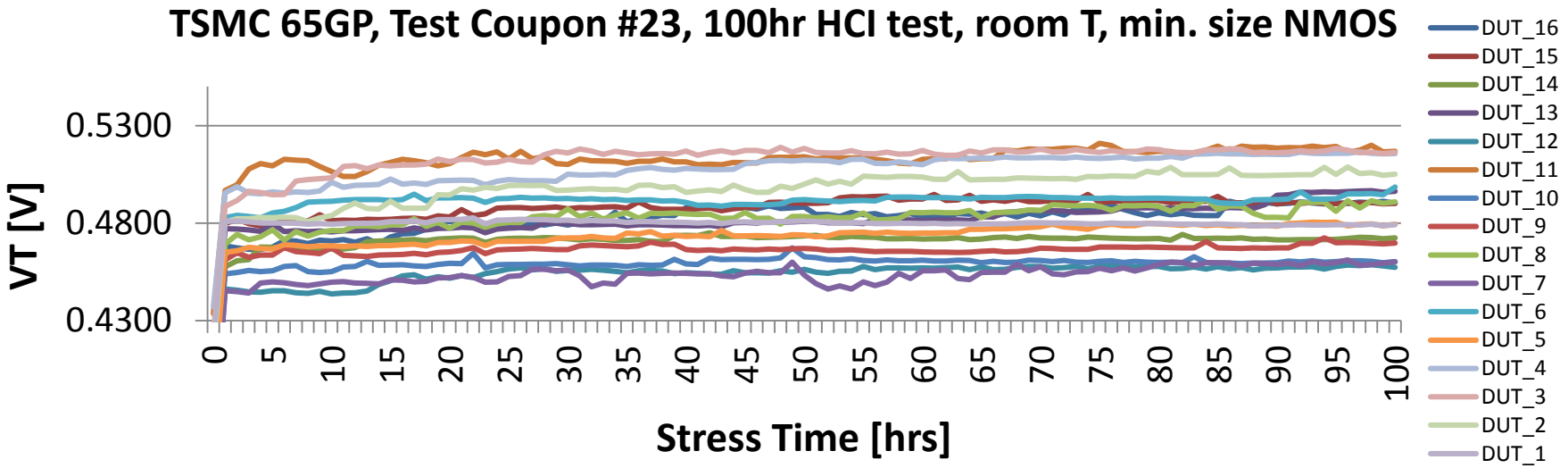
## Via Electromigration & Stress Migration – VIA EM/SM [vias &metal structures]

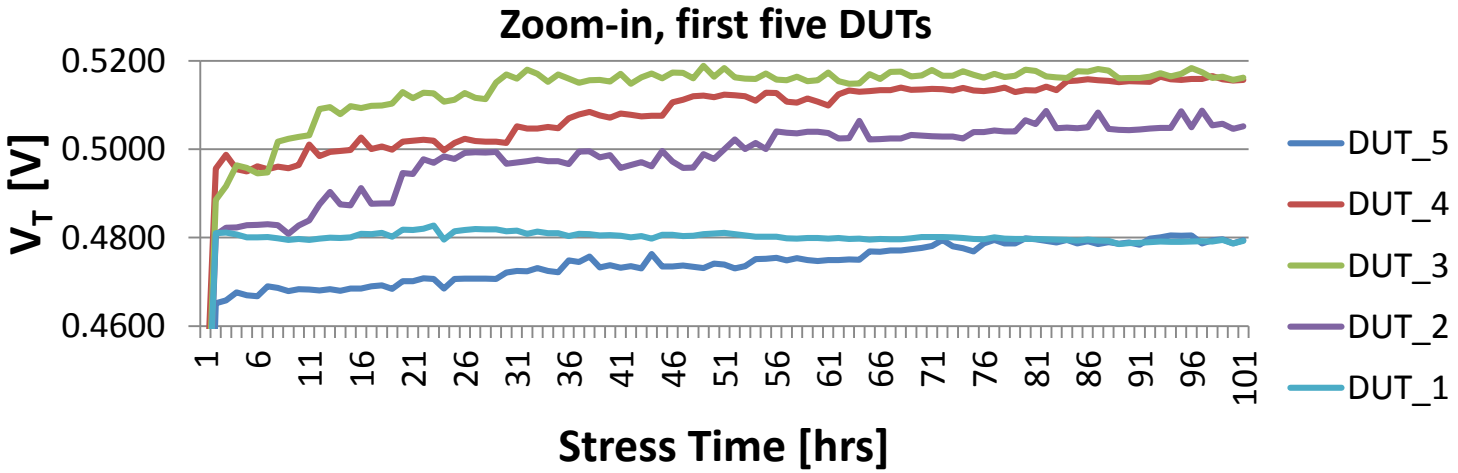
- Vds and Ids are measured for a DC bias of the Drain-Source terminals.
- DUTs are measured at a programmable frequency, duration, and test temperature.

# ProChek Software Interface

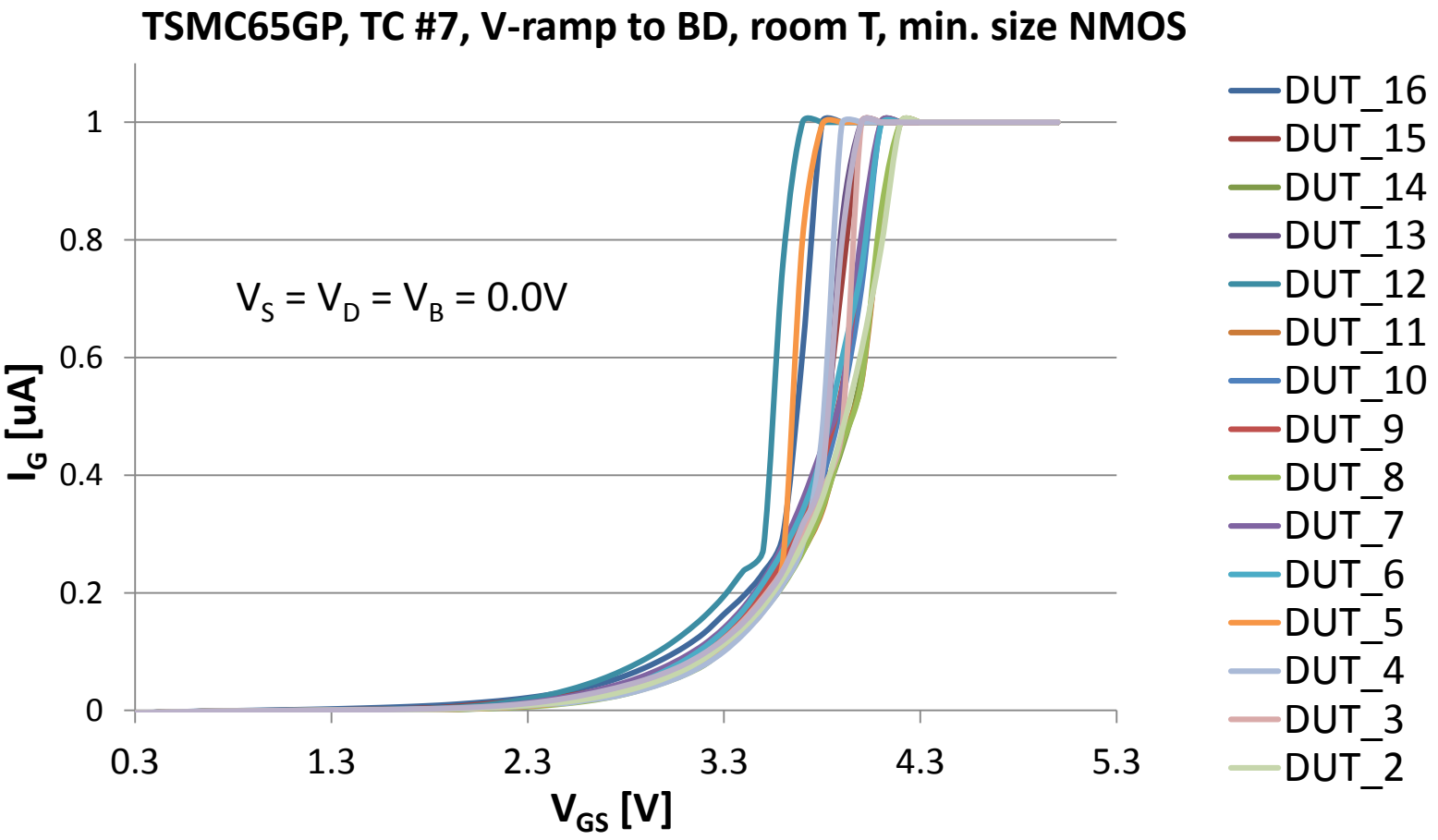


# HCI ProChek Test Results



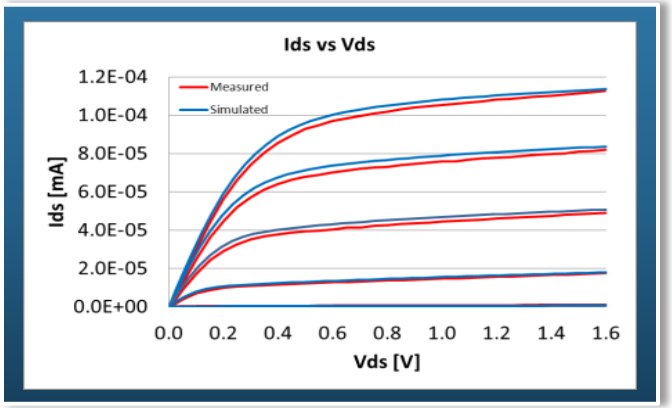



# ProChek Test Results: V-ramp to Breakdown



# Foundry PDK May Not Be Sufficient

| Reliability Concerns | Foundry PDK | ProChek |
|---|---|---|
| Variations Across Wafers & Lots | | ■ |
| Application-specific effects (e.g., temperatures, radiation, biasing, specific geometries) | | ■ |
| Physical fabrication effects (e.g., directional, wafer angle) | | ■ |
| Random parameter fluctuation simulation data | | ■ |



# Summary

## ProChek

Advanced, dedicated system for fabrication process characterization offering significant advantages to IC designers, process, and reliability engineers.

- Covers reliability concerns of modern nanotechnology processes, including radiation effects
- Covers qualification needs for new and immature processes
- Significant cost and time savings

# Contact Information

## Ridgetop Group Inc.

**Dr. Hans Manhaeve**
CEO, Ridgetop Europe
Hans.Manhaeve@Ridgetop.eu

3580 West Ina Road
Tucson, AZ 85741

# Upcoming Webinars

| Topic | Date | Time |
|---|---|---|
| Reliability Challenges in Through-Silicon Via (TSV)-Based Packaging | August 13, 2014 | 8:00 – 9:00 AM PDT |
| Radiation Shielding Design, Analysis, and Optimization | September 10, 2014 | 8:00 – 9:00 AM PDT |
| Intermittent Fault Detection in Circuit Boards and Connectors | October 8, 2014 | 8:00 – 9:00 AM PDT |

**For more information about Ridgetop Group webinars, email us at information@ridgetopgroup.com**

# Questions?

- Slides and recording of the webinar will be available shortly via an e-mail from Ridgetop
- E-mail follow-up questions & comments to hans.manhaeve@ridgetop.eu
- Please fill out our brief feedback survey at https://www.surveymonkey.com/s/QZNQDW5

Thanks for your time and interest!