Ridgetop Group Inc

ENGINEERING INNOVATION IN ELECTRONIC PROGNOSTICS

Electronic Prognostics

Solder Joint Built-In Self-Test™ A (SJ BIST™ A)

Industry-Standard, High-Performance, Electronic Prognostic Technology

- Built-In Self-Test IP Core detects incipient fatigue damage to dedicated pins of FPGA packages, especially BGA packages
- Detects damage prior to catastrophic failure of FPGA
- Improves fault coverage without significantly increasing complexity of system
- Improves fault coverage for Advanced Redundancy Management without using redundancy techniques
- Provides positive correlation of hardware faults to intermittencies

General Description

Solder joints within field programmable gate arrays (FPGAs) in Ball Grid Array (BGA) packages are especially subject to cumulative fatigue damage. Prior to development of Ridgetop's Solder Joint Built-In Self-Test™ (SJ BIST™) product, there were no known methods for detecting high-resistance faults in functional solder-joint networks in programmed FPGAs. The cumulative damage eventually causes the solder joint to crack, usually at the package or PWB boundary (Figure 1).

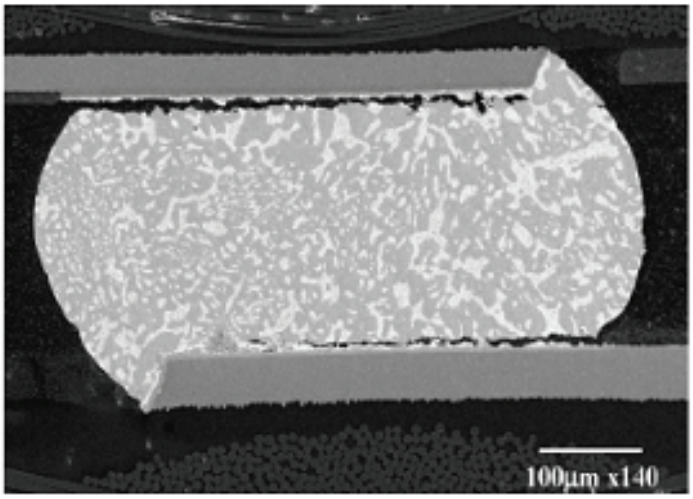

Figure 1: Cracked solder ball on the verge of fracturing (from Lall)

Revision 1.0 (09-2009)

SJ BIST is designed to detect occurrences of high-resistance spikes at BGA pins and to then alert the system regarding the condition of the solder joints. Maintenance is thus facilitated, either through replacement or by switching to a redundant system prior to catastrophic failure.

An example of a fine-pitch BGA assembly is the XILINX® FPGA FG1156 shown in Figure 2: the solder balls have a pitch of 1 millimeter and a nominal ball size of 0.60 millimeter.

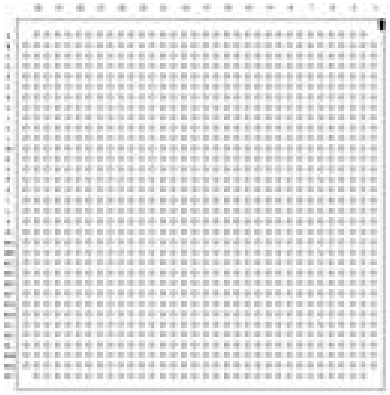

Figure 2: XILINX FG1156 Footprint – 1156 solder balls in a 34 x 34 array with a 1 mm pitch

Thermal stress and physical stress are primary causes of solder-joint fatigue damage. Thermal-related damage results from differences in the coefficients of thermal expansion of the materials in the FPGA, solder, wiring, interconnections, and printed wire board (PWB), as well as from heating and cooling due to ambient temperature changes and to power on-off cycling.

Physical stresses and strains result from shock, vibration, and torque forces to which the assembled PWB is subjected during missions, maintenance, and storage. The cumulative damage eventually causes the solder joint to crack, usually at the package or PWB boundary.

Figure 3 shows spikes of high resistance (loss of continuity) that occurred when an assembly was subjected to strain from mechanical shock waves.

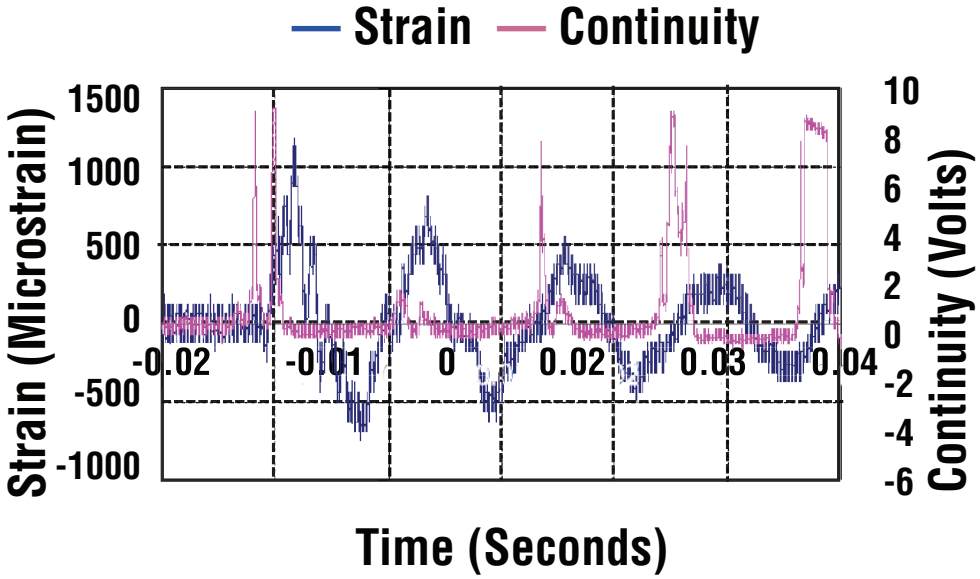

Figure 3: Strain in the form of mechanical shock waves and resultant intermittent solder bump faults

SJ BIST Features

Over time, more solder balls crack and fracture, existing fractures stay open longer, and contamination layers build up between the surfaces of fractures.

The damaged solder joints typically manifest themselves by intermittent increases (spikes) in the resistance of the network from milliohms to tens of ohms or more, and high-resistance spikes of increasing frequency and duration.

As solder-joint network faults tend to be intermittent in nature, they are difficult to diagnose. Often, when a removed assembly or board is examined and bench-tested, “No Trouble Found” (NTF) is the diagnosed code. Explanations for this include:

1. Bench tests typically do not include thermal cycling, shock, and vibration.

2. Visual inspection, with or without magnification, is ineffective because the solder balls are very close together and shielded from viewing.

3. Bench-oriented tests are a post-mortem activity performed after the assembly and the FPGA on it are suspected of being the cause of some malfunction.

The resistance of a solder-joint network in an I/O port of a programmed, operational FPGA cannot be measured directly because of the input and output buffer circuitry of an I/O port.

SJ BIST enables early detection and identification of an assembly likely to experience a malfunction. The prognostic is programmed into the FPGA and a small capacitor is attached to selected, unused I/O pins, which are monitored or tested by SJ BIST.

While a particular damaged solder-joint port might not result in immediate FPGA operational failure, the damage indicates the FPGA is no longer reliable. The occurrence of even a single fault is a prognostic warning: to avoid a near-term operational intermittent or long-lasting fault, maintenance is required.

The early detection possible with SJ BIST allows corrective actions using condition-based maintenance (CBM) procedures to be performed, and operational failures avoided.

In addition to prognostics, SJ BIST can be used in newly designed manufacturing reliability tests to investigate failure modes related to the PWB-FPGA assembly.

Technical Specifications

State-Driven Program Logic

SJ BIST uses a 5-bit, state-driven program logic to control both the current state and the writing of pins simultaneously.

SJ BIST Input and Output Signals

The SJ BIST core has the following input signals:

1. clk – FPGA clock

2. enb – Active high, level sensitive, to start SJ BIST.

3. rst – Active high, level sensitive, to reset output error signals and counts.

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The SJ BIST core has the following output signals:

1. err_indication1 – Active high, indicates a fault has occurred on the first of two I/O ports.
2. err_indication2 – Active high, indicates a fault has occurred on the second of two I/O ports.
3. ps1 – Active high, indicates a present (current) fault on the first I/O port.
4. ps2 – Active high, indicates a present (current) fault on the second I/O port.
5. err_count1, 8-bit count [7:0] of the number of fault detected on the first I/O port.
6. err_count2, 8-bit count [7:0] of the number of faults detected on the second I/O port.

Number of Logic Elements in a 4-core, 8-pin SJ BIST Implementation

220 to 400

Estimated Power to Monitor 8 Pins

The estimated power to monitor pins is dependent on the driving current of the I/O ports of a specific FPGA. For a XILINX FG1156, Spartan 3 series, the estimated power to monitor 8 pins is 150 mW maximum.

Soft Core Design

- No false alarms at test frequencies of 1, 10, and 20 MHz.
- Guaranteed detection duration reduced to 2 clocks – 200 nanoseconds at 10 MHz and 40 nanoseconds at 50 MHz.
- Depending on when the fault occurs, a 50-nanosecond fault is detectable. The detection resolution of 50 to 200 nanoseconds compares favorably with a manufacturing reliability standard of 1,000 nanoseconds.
- The detection sensitivity is as low as 100, which compares favorably with a manufacturing reliability standard of 300.

Two-Port Test Results

Figure 4 shows the signal across an external capacitor for 1 MHz clock, no fault and fault. No false alarms occurred. Figure 5 shows the timing.

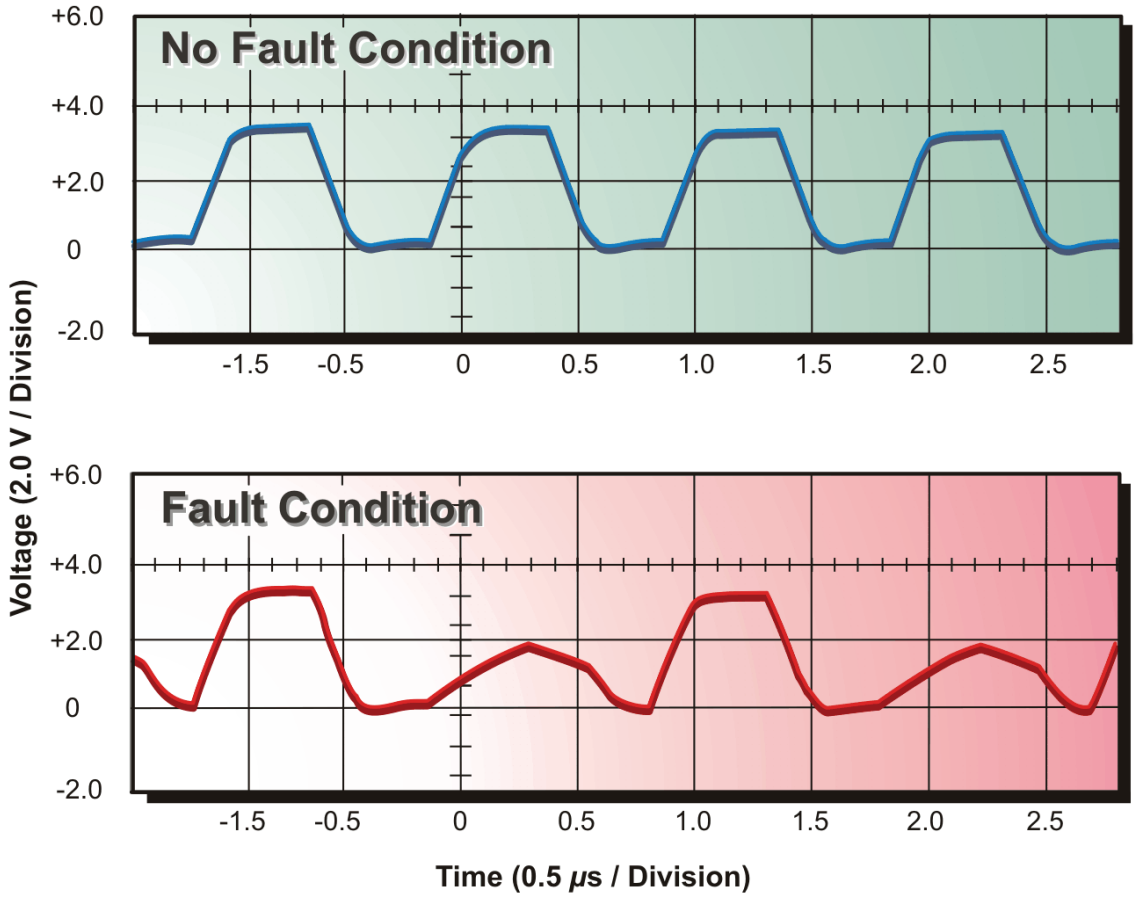

Figure 4: SJ BIST two-port test, 1 MHz clock

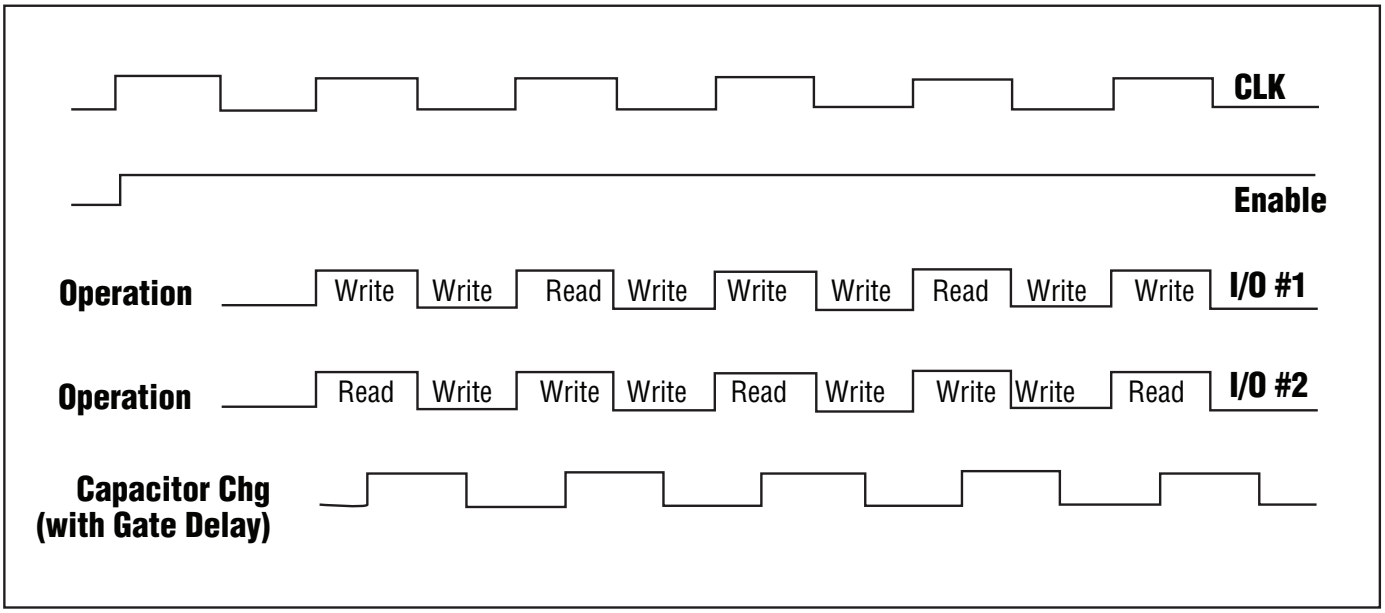

Figure 5: SJ BIST timing diagrams

FPGA Clock Frequency and RC Relationship

Figure 6 is a family of clock frequency curves showing the resistance-capacitance (RC) relationship. From left to right, the plots correspond to clock frequencies of 20 MHz, 10 MHz, 1 MHz, and 100 kHz.

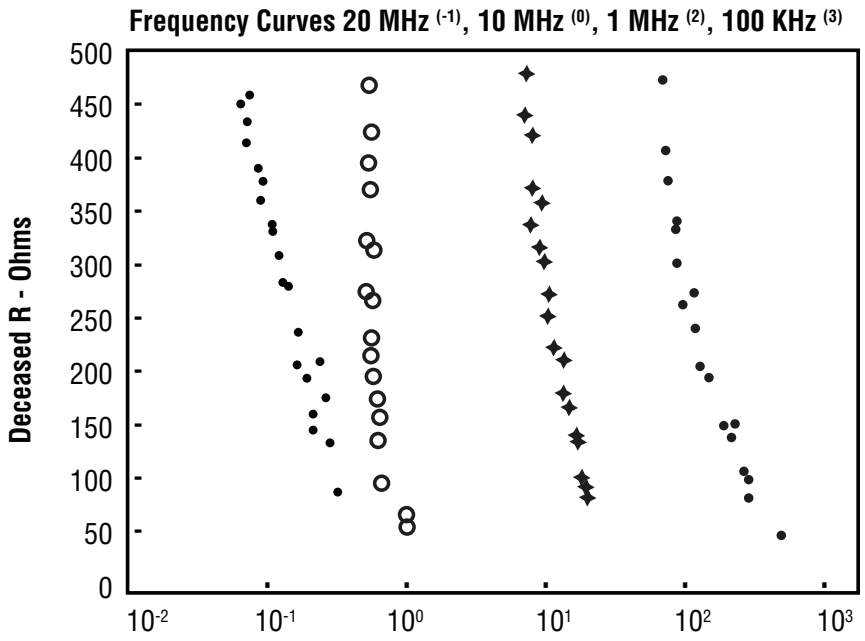

Figure 6: Family of clock frequency curves showing RC relationship

Customer Testimonial

"SJ BIST is the first known direct in-situ measurement that is a true canary for intermittent electrical contact between bumps, PCB, and package."

— German Automotive Firm

Need modified or custom design? Contact Ridgetop at 520-742-3300 to discuss your ideal solution!

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