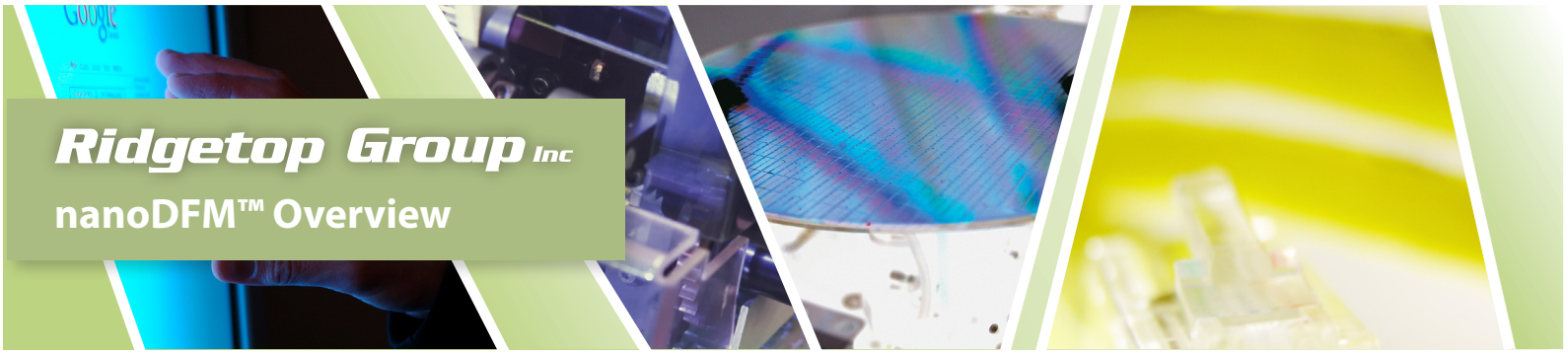


nanoDFM™ Technologies

Design-for-Manufacturing Tools for High-Performance ICs

What is Design for Manufacturing or DFM?

The success of nano-level integrated circuits depends on the integration of advanced methodologies throughout the entire semiconductor process development cycle. Ridgetop Group's nanoDFM™ product suite is designed to provide that level of integration, to combat yield losses stemming from process-related and design-related problems.

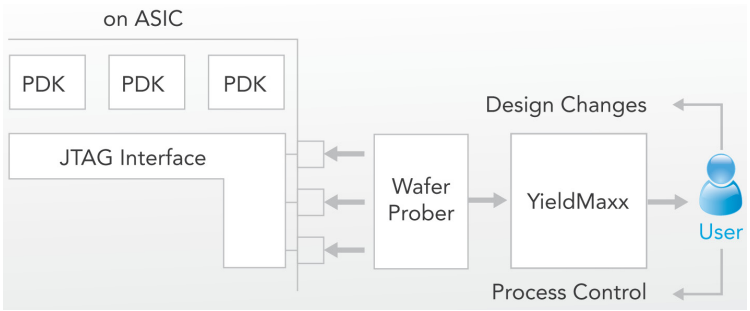
Ridgetop's nanoDFM technologies apply advanced and patented in-situ test structures and iterative improvements. By providing performance metrics and electrical testing, useful lifetime is increased and yields improved. To do this, the most sensitive circuits must be identified as well as the mechanisms likely to have negative effects.

Yield Losses

It is estimated that at 65 nm, design-related yield losses can reduce overall yields by 30%. Undoubtedly, this is one of the reasons the ramp-up to 90 nm production has taken over two years and the 65 nm ramp-up may take three years as compared to the one and a half years taken for 130 nm.

At Ridgetop Group, we develop families of intelligent, design-for-manufacturing tools covering the entire semiconductor development lifecycle. Our nanoDFM technologies provide techniques to improve the yield, design processes, and reliability of emerging nano-level processes for fabless and fab manufacturers.

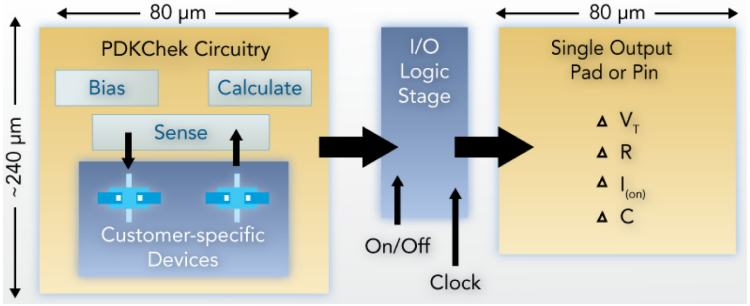
These solutions are part of a suite of prognostic tools covering electronic devices from in-situ test structures on silicon to asset tracking software tools that manage across the globe.



Centered Design for Optimizing Field Life

Features & Benefits

- Mismatch measurement of threshold voltage, V_T
- Nano-level (sub-90 nm) measurement of feature size transistors
- Mismatch measurement of resistance and capacitance
- Die-to-die variation analysis
- Long-term reliability and variation analysis
- Extensibility
- Digital output (option)



PDKChek® Implementation

Ridgetop Group Inc

ENGINEERING INNOVATION

Features	Advanced Effects
Mismatch Measurement of Threshold Voltage	
PDKChek® supports individual transistor characterization for the specific lengths and widths chosen, and at the specific bias points that are used.	• Excessive threshold mismatch can cause timing errors in digital circuits or gain errors in analog circuits. • Large numbers of PDKChek structures can be used across the wafer to obtain process-dependent statistics.
Flexible and Integrated Interface	
PDKCheck YieldMaxx™ software utility is a statistical analysis tool designed specifically for the interpretation of wafer-variation data.	• Detect, analyze, and correct process-related and design-related issues. • Easily integrated GUI provides unparalleled visibility and analysis of chip design and integrity while on the wafer. • Schmoo plot, thermoanalysis, geometrical cross-sections. • Statistical parameter analysis. • Improved intrawafer and wafer lot visibility and analysis.
Nano-level (Sub-90 nm) Measuring of Feature Transistor Size	
To ensure high levels of reliability and performance, prognostics technology developers must analyze prognostic data for intermittent fault detection, root cause analysis, and health management.	• Prognostic systems and tools dedicated to detecting intermittent faults, performing root-cause analysis, and implementing intelligent health management activities. • Sensor-rich platforms designed to use existing operands and measurands for correlation with access to PCI / VME buses.
Analysis for Resistors and Capacitors	
PDKChek supports individual parameter characterization for the specific dimensions chosen, and at the specific bias points that are used.	• Allows design to reach extremely high data resolution, providing optimal performance and linearity for data converters.
Die-to-Die Variation Analysis	
As a die-level monitor, PDKChek can be used to compare variations in threshold voltage, resistance and capacitance across the wafer.	• More accurate means of examining hard-to-obtain data.
Long-Term Reliability and Variation Analysis	
Since PDKChek stays with the die and IC, the structure can be probed for long-term reliability and lifetime testing purposes.	• More accurate means of examining hard-to-obtain data.
Digital Output (option)	
PDKChek offers an optional method of digitally extracting the data using a standard IEEE 1149.1 JTAG scan bus interface.	• Fits easily into semi-automated test paradigm. • Increases I/O performance. • Improved internal signal integrity.

Ridgetop Group may from time to time make changes to the products or specifications contained herein without notice.
The Ridgetop Group nanoDFM™ technologies and PDKChek® are covered by U.S. patent 7,239,163 and other issued and pending patents.

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