



ADC 10-bit, 4 MS/s, TSMC 0.25 μm IP Core

Semiconductor IP



Industry-Standard, High Performance, Silicon-Proven ADC Technology

- 10 bits of resolution
- 4 MS/s sampling rate
- TSMC 0.25 μm mixed-signal process (retargetable)
- 3.0 to 3.6 V analog supply voltage
- 2.25 to 2.75 V digital supply voltage
- Area 1.25 x 1.5 mm (TSMC 0.25 μm process)
- Pin provided for enable mode
- External (or internal) reference voltage
- Up to 10 analog inputs
- MIM capacitors
- Pipeline architecture
- Includes complimentary license of patented PDKChek[®] die-level process monitor yield improvement solution

General Description

Ridgetop Group's 10-bit, 4 MS/s ADC core utilizes a pipeline architecture in the TSMC 0.25 μm process. The ADC converter design is 10-bit 4 MS/s, as shown in Figure 1.

The cell incorporates a 10-bit pipeline analog-to-digital converter with up to five sample-and-hold blocks. Four sample-and-hold blocks are used in parallel to sample input voltage and current. The fifth sample-and-hold block is used with the input multiplexer to provide up to eight auxiliary inputs. The cell also includes a current-to-voltage converter that converts current input signals to voltages.

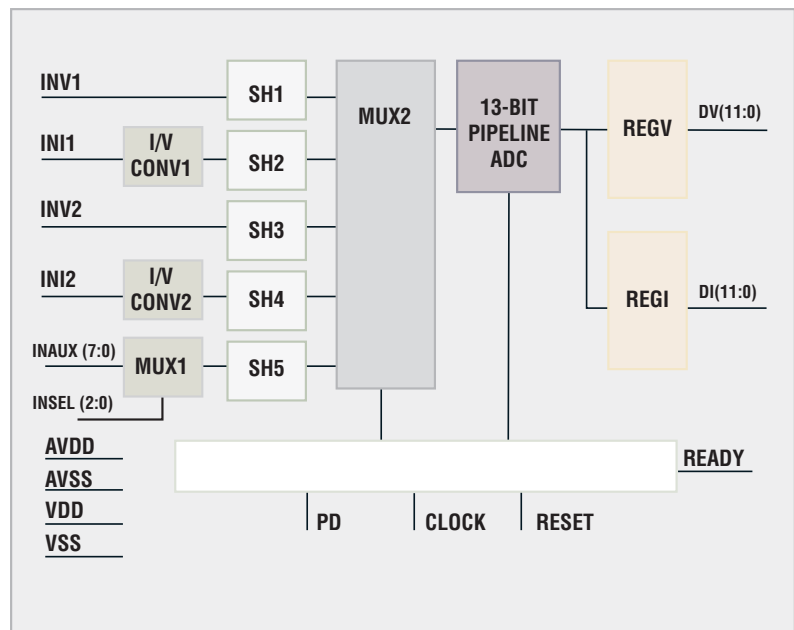


Figure 1: ADC design, block diagram

Applications

- Commercial communications
- Consumer electronics
- Instrumentation
- Video

Table 1: Operating Conditions

| PARAMETER | MIN | TYPICAL | MAX | UNITS |
|------------------------------|------|---------|------|-------|
| Analog Power Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| Digital Power Supply Voltage | 2.25 | 2.5 | 2.75 | V |

Table 2: Absolute Maximum Ratings

| PARAMETER | MIN | MAX | UNITS |
|------------------------------|------|----------|--------|
| Analog Power Supply Voltage | -0.3 | AVDD+0.3 | V |
| Digital Power Supply Voltage | -0.3 | VDD+0.3 | V |
| Analog Input Voltage | -0.3 | AVDD+0.3 | V |
| Junction Temperature | -65 | 150 | Deg. C |

Table 3: Electrical Characteristics

| PARAMETER | MIN | TYPICAL | MAX | UNITS |
|------------------------------|----------|---------------|----------|-------------|
| Resolution | | 10 | | Bits |
| Analog Input Voltage | 0 | tbd | AVDD | V |
| Analog Input Current | -1 (tbd) | tbd | +1 (tbd) | mA |
| Sample Rate | 1 | 4 | 6 | MSPS |
| Data Latency | | 8 | | Clock Cycle |
| Input Clock Frequency | 1 | 4 | 6 | MHz |
| Input Clock Duty Cycle | 40 | 50 | 60 | % |
| Integral Nonlinearity | | ±1 | ±2 | LSB |
| Differential Nonlinearity | | ±0.8 | ±1.2 | LSB |
| Signal-to-Noise Ratio | | 64 (at 2 MHz) | | dB |
| Offset Voltage | -8 | 0 | 8 | LSB |
| Digital Input Low Voltage | 0 | - | 0.8 | V |
| Digital Input High Voltage | 1.7 | - | VDD | V |
| Analog Power Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| Digital Power Supply Voltage | 2.25 | 2.5 | 2.75 | V |

Table 4: Cell Pin Definitions

| PIN | DESIGNATOR | INPUT/OUTPUT/POWER | DESCRIPTION |
|-----|-------------|--------------------|--|
| 1 | AVDD | P | Analog Power Supply |
| 2 | AVSS | P | Analog Power Ground |
| 3 | VDD | P | Digital Power Supply |
| 4 | VSS | P | Digital Power Ground |
| 5 | CLOCK | I | Clock Input |
| 6 | PD | I | Power Down Control Input. When in logic level one, ADC and all circuitry are in Power Down Mode. |
| 7 | INSE [2:0] | I | Auxiliary Input Select control code |
| 8 | INV1 | I | Voltage Input 1 |
| 9 | INV2 | I | Voltage Input 2 |
| 10 | INI1 | I | Current Input 1 |
| 11 | INI2 | I | Current Input 2 |
| 12 | INAUX [7:0] | I | Auxiliary Inputs |
| 13 | DV [11:0] | O | Voltage Output Data |
| 14 | DI [11:0] | O | Current Output Data |
| 15 | READY | O | Data Ready Output. Output data should be sampled at logic level one on this pin. |
| 16 | RESET | I | Digital Circuitry Reset Control |

Technical assistance will be provided for integration of this IP.

Need modified or custom design? Contact Ridgetop at 520-742-3300 to discuss your ideal solution!

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