

Time-Dependent Dielectric Breakdown (TDDDB) Prognostic BIST Cell™

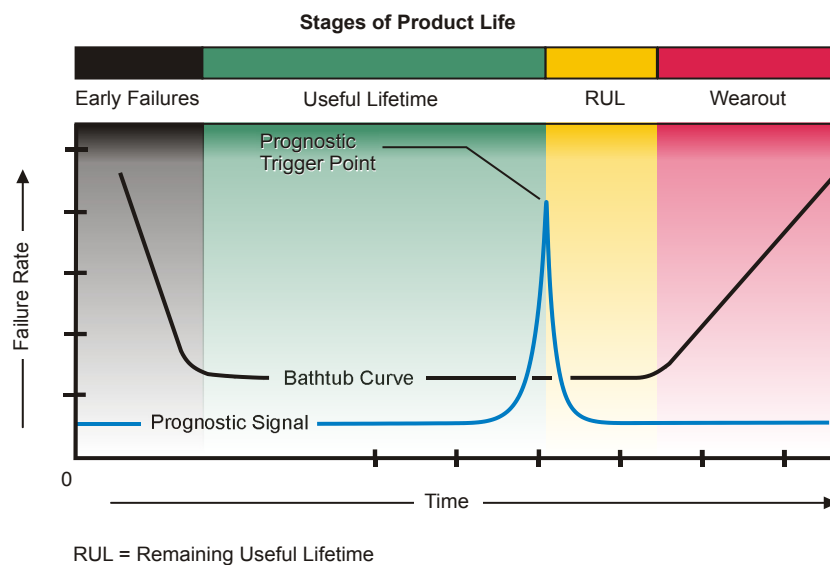
Electronic Prognostics



Industry-Standard, High-Performance, Prognostic Cell Technology

- The Ridgetop TDDDB Prognostic Built-in Self-Test (BIST) cell acts as an early-warning “sentinel” of an upcoming gate oxide failure condition due to Time-Dependent Dielectric Breakdown (TDDDB)
- Size: 500 μm^2 at the 0.13 micron process size
- Prognostic “distance” breakdown can be scalable using design equation
- Power consumption is approximately 600 microwatts
- Detects both hard and soft breakdowns

General Description Ridgetop’s TDDDB Prognostic BIST Cell is a pad-limited CMOS leakage detection cell. Its unique and proprietary architecture behaves as an early-warning “sentinel” of upcoming gate oxide failure. The amount of pre-warning is dependent on the prognostic distance, which depends on the area and the stress voltage.



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Figure 1: Reliability bathtub curve

The TDDB cell is designed to be co-located with the host circuit and subjected to the same environmental stresses. These environmental stresses contribute to aging of the circuit and can include over- and under-voltage conditions, transient spikes, radiation exposure, humidity, and excessive temperature conditions.

The TDDB prognostic cell is approximately $500\text{ }\mu\text{m}^2$ at the 0.13 micron process size. The cell is co-located on the same substrate as the host circuit, and shares the power and physical environment for optimum tracking of the aging effects. Estimated power consumption of the cell is approximately 500 microwatts.

Prognostic Distance

The Prognostic Distance is adjusted by scaling the area of the cell. Ridgetop has nominally set this at 80% of the statistical end-of-life point. This point can be adjusted to some other early indication level. A “picket fence” can also be constructed with multiple cells evenly spaced over the bathtub curve (Figure 1).

Figure 2 shows the TDDB block diagram; Figure 3 shows failure distribution in a HALT; Figure 4 shows soft and hard breakdown with voltage vs. oxide resistance; and Figure 5 shows a sample TDDB cell layout.

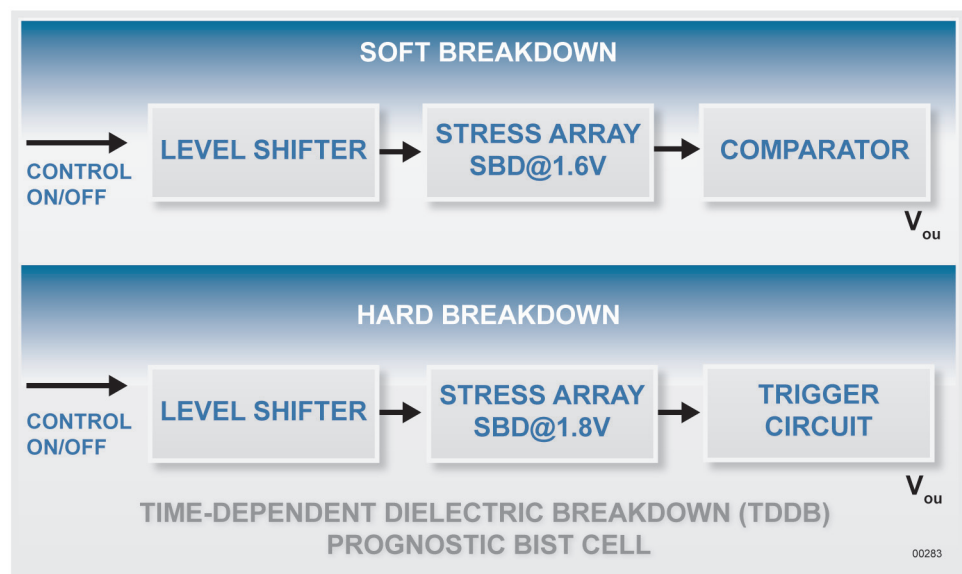


Figure 2: TDDB block diagram

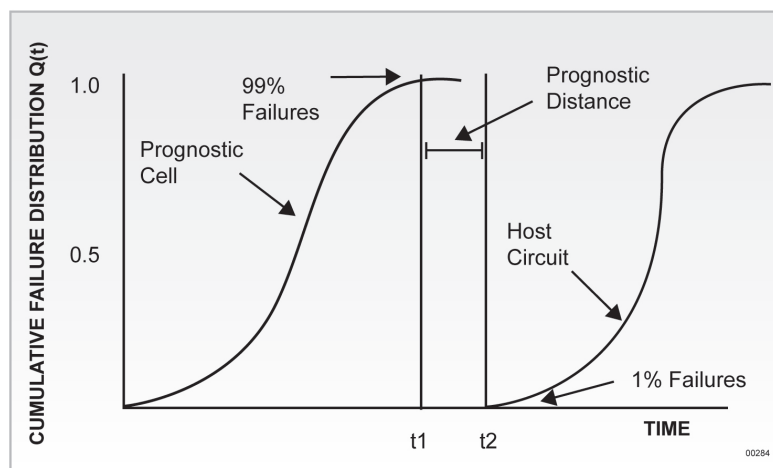


Figure 3: TDDDB cumulative failure distribution in Highly Accelerated Life Test (HALT)

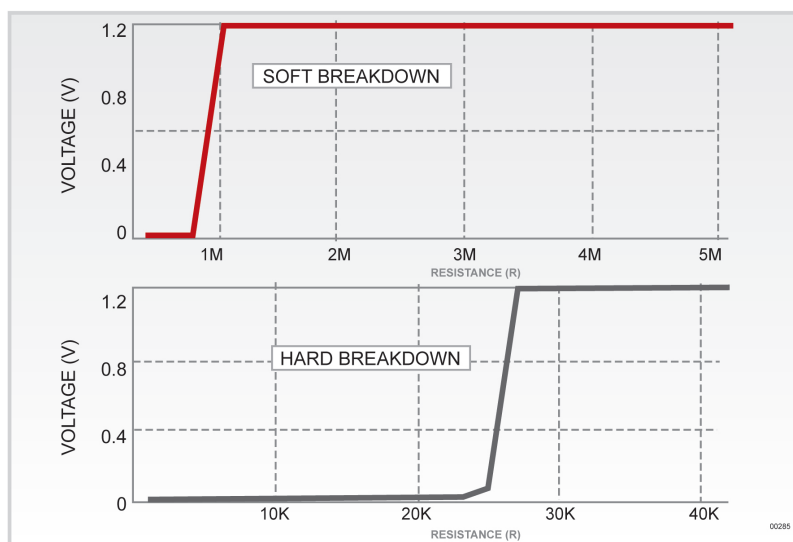


Figure 4: TDDDB simulation of soft breakdown and hard breakdown, showing voltage vs. oxide resistance

Interfacing

The TDDDB cell, as well as other prognostic cells in the Sentinel™ network, can be configured for a simple buffered logic high or low output to indicate an impending failure event.

Optional Interfacing using the JTAG Bus Structure

Using the JTAG toolkit, it is also possible to include a register in a chip design that permits an interface using the standard scan test bus that employs IEEE-1149.1. This interface uses four control lines:

TDI - Test Data In

TDO - Test Data Out

TCK - Test Clock

TMS - Test Mode Select

If the JTAG toolkit is utilized, the prognostic cell uses the TDO and TMS lines. The TDO changes its logic state upon a detected failure event and the TMS is used to invoke a “self-test” function to ensure that the cell is functional.

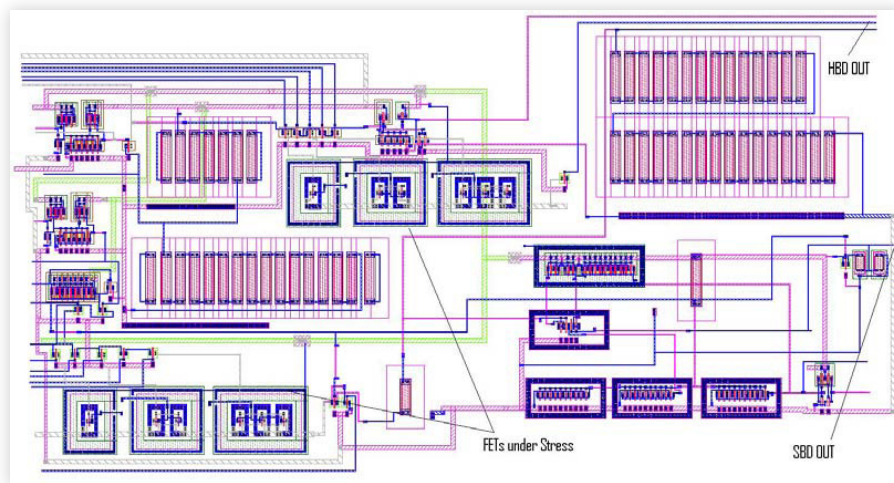


Figure 5: GDSII Layout of Tddb cell to detect hard and soft breakdown

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