For Immediate Release…

PDKChek™ Process Verification IP

Introduced for Fabless IC Houses

Grenoble, France – December 8, 2004

Ridgetop Group, Inc. announced today PDKChek™ IP, the first in a line of IC level process verification products for Fabless Semiconductor Manufacturers. The announcement was made at the IP/SoC Conference in Grenoble, France.

Fabless Semiconductor Manufacturers rely upon process-dependent data supplied by external Semiconductor Foundries to create accurate and well-centered IC designs. The supplied foundry data is contained in Process Design Kits (PDK's). When the actual process variations differ from the PDK's, then the ICs will not work properly, if at all. Some Fabless IC companies have reported costly development delays as disputes occurred between the foundry and the Fabless IC design team on problems that turned out to be foundry-related. As process geometries continue to shrink, there have been wide variations reported in MOS device performance, especially mismatch, exacerbating the problem (See the attached Mismatch Sidebar).

Based on these issues, Ridgetop conducted a multiyear development effort to create a line of low-cost calibrated test structures (PDKChek™) that can be employed to verify compliance with the PDK's at the Die Level. The first in this line of structures provides direct and calibrated measurement of device mismatch, a key performance parameter for analog/mixed-signal IC designs. The PDKChek™ structures are quite small (150 µm by 100 µm) and are co-located with the host IC design. This approach provides a simple and effective independent measure of mismatch using patent-pending techniques developed by Ridgetop.

According to Doug Goodman, Ridgetop's CEO, "As a Fabless IC firm ourselves, we have found PDKChek™ to be an effective tool to assure that foundry-supplied design constraints are accurate, especially dealing with

mismatch. With shorter development timelines, this is critical to meeting our customer commitments. We call this the “trust, but verify” strategy”.

About Ridgetop Group, Inc.

Ridgetop introduced the industry's first independent Die Level Process Monitor solution, PDKChek™ for nanometer designs. Established in 2000 in Tucson, Arizona, Ridgetop has supplied advanced mixed signal designs for a variety of demanding customers such as NASA, Navy and the Missile Defense Agency.

Corporate headquarters are located at 6595 North Oracle Road, Tucson, Arizona 85704.

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Mismatch sidebar

In a semiconductor-manufacturing environment, fluctuations in device parameters result from the inherent random nature of processing. Deviations of these process-related parameters from their nominal values cause differences in device performances between identically designed transistors, referred to as mismatch. Process related contributors to MOS mismatch include non-uniformity of dopant atoms in the depletion layer, dimensional variations, interface states, etc.

Identical electronic components are important for accurate small signal processing. An example of a practical application of MOS transistors for analog design is the differential pair consisting of two adjacent identically designed transistors shown in the circuit-level diagram in Figure 1. Mismatch between transistors is a dominant factor affecting circuit performance, usually amplified in subsequent circuit gain stages. Mismatch effects are inversely proportional to transistor area and therefore become increasingly important as the dimensions of the transistors are reduced.

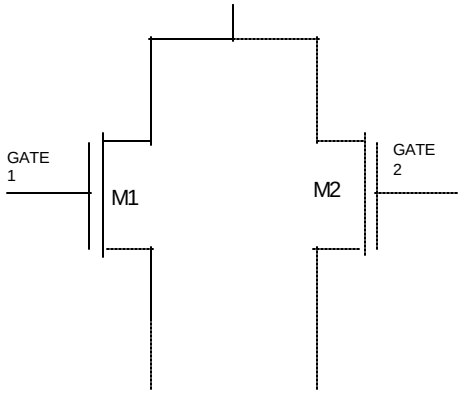

Figure 1: Differential MOSFET pair consisting of two adjacent identically designed transistors.