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SiliconAid Solutions evolves support of IEEE P1687 and IEEE 1149.1-2013 Standards through Partnership with Ridgetop Group

Seattle, WA — October 20, 2014

SiliconAid Solutions, Inc., and Ridgetop Group., announced jointly today they have continued and expanded their partnership to enable support for the evolving industrial testability standards. Together they have developed a system to embed Ridgetop Group's SJ BIST™ board-level interconnection reliability monitor leveraging IEEE P1687 and IEEE 1149.1-2013 for intellectual property (IP). SJ BIST is a patented test IP product that detects interconnect faults between electronic devices, such as between integrated circuits (ICs) (including field programmable gate arrays [FPGAs] and systems-on-chip [SOCs]) and printed circuit boards (PCBs).

Ridgetop and SiliconAid applied SiliconAid's IEEE 1149.1-2013 and P1687 tool flows to develop compliant access to SJ BIST IP. Ridgetop continues to be a partner/customer to test and verify the SiliconAid IEEE 1149.1-2013 and P1687 flows. These adjusted implementations leverage enhanced automation, reuse, and debug capabilities of embedded chip instruments. In the past, a significant manual effort has been required to verify that embedded instruments were integrated and verified correctly in the customer design. Procedural Description Language (PDL) test pattern generation also had to be handled by the IP integrator. Using SiliconAid's new flow, a custom testbench can be generated automatically for every design in which the IP is used. Chip-level automated test equipment (ATE) patterns can also be generated automatically.

According to Andrew Levy, Ridgetop's VP of Business Development, "SJ BIST offers a solution for detecting troublesome intermittencies. We have worked with SiliconAid to take Ridgetop's SJ BIST Test IP Core through their P1687 IJTAG and boundary scan flows. Now that we have developed and demonstrated the ability to convert legacy patterns to PDL patterns that can be applied with these interface, our customers will enjoy even faster and more flexible deployment of SJ BIST to meet their needs for highly reliable boards and systems."

Jim Johnson, SiliconAid President and CTO, added, "We believe all IP providers will soon be delivering with support for both P1687 and 1149.1-2013 to enable IP reuse. The Plug and Play approach used by these new standards is a perfect fit for an IP provider like Ridgetop to improve quality and help the chip integrators. Utilizing these new standards will reduce the cost of integration, verification, and test pattern generation for the SOC companies using the IP. We support both of these two new standards and have a robust suite of tools to meet your needs for IP developers, SOC integrators, verification, manufacturing test, debug, and more."

Ridgetop Group and SiliconAid Solutions invite you to see a demonstration of the new capabilities and learn more at booth #604 at the International Test Conference in Seattle, Washington, October 21-23, 2014.

About Ridgetop Group, Inc.

Established in 2000, Ridgetop Group is a Tucson, Arizona-based firm that produces electronic solutions for harsh environments and challenging applications. The firm is qualified as an aerospace supplier under its AS9100C certification, and became a Category 1A Trusted Supplier under the DoD's Trusted Foundry Program in 2010. A privately held firm, Ridgetop operates two divisions in Tucson, and has a related subsidiary firm based in Europe near the European Space Agency facilities.

For more information, please contact information@ridgetopgroup.com or visit Ridgetop's website at www.ridgetopgroup.com.

About SiliconAid Solutions

SiliconAid Solutions, Inc. is recognized as a leading provider of Design for Test Consulting and for world class chip-focused JTAG software solutions to validate, verify, and utilize IEEE JTAG-related industry standards. SiliconAid has corporate headquarters located in Austin, Texas and was founded in 2001. The Consulting Product Group has been recognized for comprehensive support of all standard EDA DFT solutions. The exhaustive chip-level validation, verification, and debug of IEEE JTAG-compliant implementations is based on over 20 years of testing and thousands of designs from multiple satisfied worldwide semiconductor companies.

For more information, please visit SiliconAid's website at www.SiliconAid.com.