Practical Application of PHM/Prognostics to COTS Power Converters

Douglas L. Goodman, Bert Vermeire
Phil Spuhler, Hari Venkatramani
Ridgetop Group, Inc.
3580 West Ina Road
Tucson, Arizona 85741
(520) 742-3300
doug@ridgetop-group.com

Abstract—An easily-adopted method of adding Prognostics/Health Management (PHM) to electronic systems is described. As an example, a PWM-type switching power supply was chosen for analysis in this paper, due to the ubiquitous nature of these Power Converters in Mil/Aero systems, and the criticality of their reliable performance.

Switch mode power supplies (SMPS) provide significant advantages to users in terms of conversion efficiency, weight, and size. According to Industry Analysts, over $7.7 Billion of SMPS Power Systems were produced worldwide in 2002. However, SMPS's have unique reliability issues when used within a system due to size constraints, heat dissipation and varying load conditions.

The internal components of a SMPS, including the Power Switch (MOSFET or IGBT), catch diode, capacitors, and magnetics are under repetitive stress conditions that contribute to elevated failure rates. Often the SMPS is considered the most vulnerable and weakest part of a system. Having an early warning of an impending failure (through PHM) would be very useful information and critical to mission success.

TABLE OF CONTENTS

1. INTRODUCTION

Prognostics/Health Management (PHM) has been described as a key element in the new Joint Strike Fighter (JSF) to reduce the overall life cycle cost of the aircraft.[3] Prognostics provides the means to predict an impending failure before it occurs, and thus can mitigate potentially catastrophic failure modes, improve the logistics support framework and increase the operational readiness of the JSF. Ridgetop has developed a methodology for Electronic Prognostics that provides deterministic techniques of failure prediction, and thus a foundation for PHM.

2. MIL/AERO ELECTRONIC SYSTEMS AND PHM

A common element for most EW and Mil/Aero systems are high efficiency power supplies. The Navy has determined a significant problem in power supplies with premature failures so this was chosen as the test case for testing the efficacy of PHM. Also, by initially focusing on such a ubiquitous component, the maximum commercial leverage could be realized from this work.

For this paper, Ridgetop selected an off-the-shelf 50 watt, DC to DC converter from a commercial power supply manufacturer, C & D Technologies. This supply was chosen due to the power supply topology being well understood and widely-used, and with the understanding that the techniques would be easily extensible to other power supply topologies and wattage sizes.

[1] 0-7803-8870-4/05/$20.00© 2005 IEEE

[2] IEEEAC paper #1628, Final Version, Updated November 22, 2004

[3] Hess, Andrew "The Joint Strike Fighter (JSF) Prognostics and Health Management" NDIA Conference, 2001

The DC to DC converter used in this analysis has the following characteristics:

Characteristic	Description
Switch Mode Power Supply (SMPS) Topology	Forward Converter Point of Load
DC Input Voltage Range	Up to 48 volts
DC Output Voltage	5 volts
Current Consumption	10 Amps
Efficiency	Up to 92%
Model Name	WPA-50
Manufacturer	C & D Technologies, Inc. Tucson, Arizona

3. PHM/PROGNOSTICS METHODOLOGY

To properly implement electronic prognostics, there are three key factors that must be understood:

- Circuit topology
- Component Failure Rate ranking
- Physics of Failure Models (precursors to failure)

This information is needed so that a suitable design can be developed and implemented for the power supply. This is a three step process is implemented as shown in figure 1.

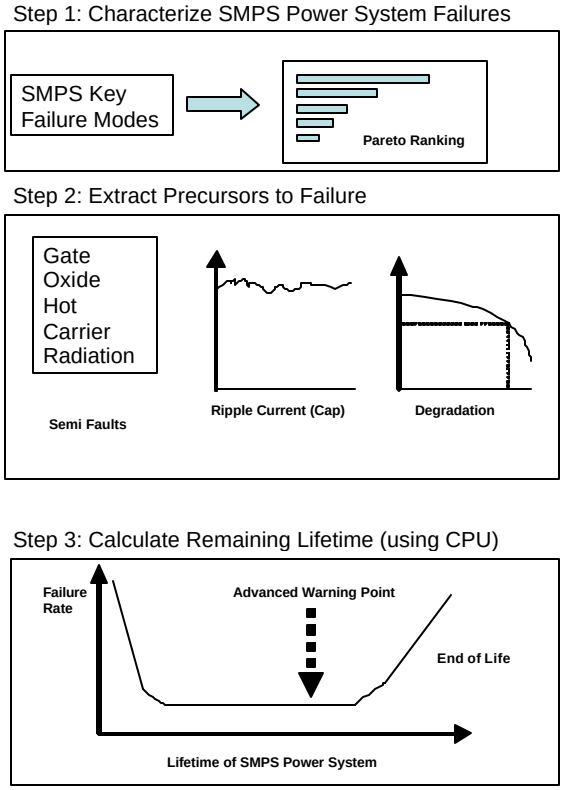


Figure 1. Electronic PHM Methodology

4. POWER SUPPLY TOPOLOGY

The WPA50 is a forward switching converter with up to 92% conversion efficiency. A simplified schematic for a forward converter is shown in figure 2.

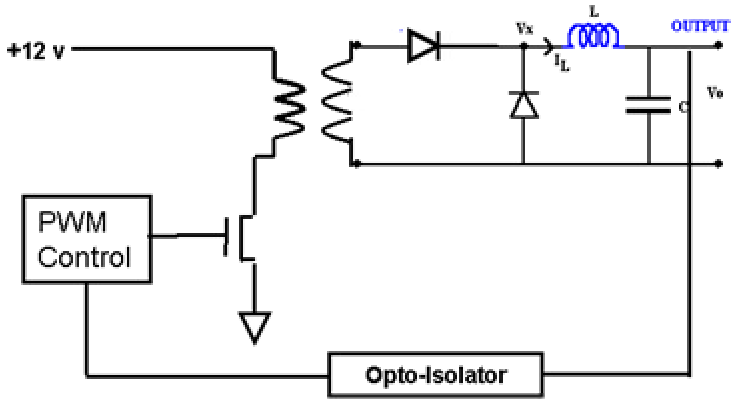


Figure 2. Simplified Forward Converter Topology

In a Forward Switching Converter, the input voltage is higher than the output voltage. Unlike a conventional buck-type converter, there is transformer that provides isolation between the primary and secondary windings. In addition to helping with the step-down requirements, the transformer can help eliminate grounding problems.

The Power MOSFET is the main power switch that is commutated by the PWM control IC. The PWM control IC samples the output via an opto-isolator so it maintains electrical isolation. The clock rate is 400 KHz and the switching and duty cycles are adjusted to maintain regulation on the output, in spite of load variations. In the actual WPA 50, the two diodes shown in the simplified schematic have been replaced by Power MOSFET's functioning as synchronous rectifiers. These components provide a higher level of efficiency than conventional power diodes.

The first step in providing a prognostic solution is to establish a Pareto Chart ranking of the components by their failure rates. C & D Technologies has an extensive database of component data, and this was used for the analysis. For the components contained in the power
supply, a ranking was developed, as shown in figure 3; this allows the developer to visually examine the most problematic components for further analysis.

5. "INSTRUMENTING THE POWER SUPPLY"

Ridgetop examined the power supply topology, along with the components having the highest failure rates. Based on this analysis, there was an examination of the physics of failure associated with each device. The reasoning is that if precursors associated with failure can be extracted, they can be processed into a meaningful prognostic for the power supply. The physics of failure give indications of impending failure modes and are a dynamic function of circuit activity and ambient conditions

As you may expect, the key components subject to degradation are the Power MOSFET's, capacitors, PWM Power IC, and the opto-isolator. For each of these components, physics-of-failure models were examined.

6. PHYSICS-OF-FAILURE MODEL DEVELOPMENT

In the examination of the Pareto Chart, the highest failure rates were found on the power MOSFET's, capacitors, opto-isolator and PWM control IC. For each device, there was a unique signature associated with degradation that leads to device failure. These models were developed and installed into Ridgetop's device library.

1st Level Root Cause	Quantity
C10/C11 SHORTED	22
D2, D3, OR D4 SHORTED	22
U2 Bad	11
Q22 Bad	9
SHORTED C7/C6	6
D25 Bad	5
D22 Bad	4
Q4 Bad	3
Q7 Bad	3
SHORTED Q3	3
C1 Bad	2
D14 Bad	2
U1 Bad	2
C23 Bad	1
C24 Bad	1
C38 Bad	1
C43 Bad	1
C51 Bad	1
C6 Bad	1
C62 Bad	1
D11 Bad	1
D27 Bad	1
D4 Bad	1
D6 Bad	1
DZ3 Bad	1
Q12 Bad	1
Q14 Bad	1
Q17 Bad	1
Q18 Bad	1
Q21 OPEN	1
Q3 Bad	1
Q5 Bad	1
Q6 Bad	1
Total Returns	114

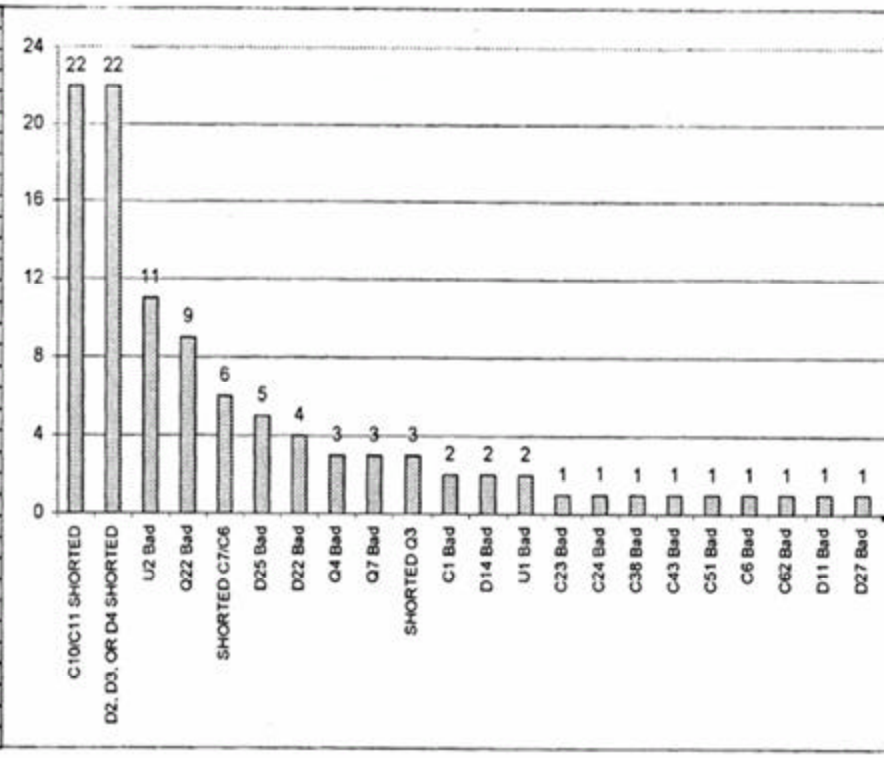


Figure 3. Pareto Ranking of Parts. With a Pareto, the highest failure rate components are on the left side of the bar chart and descend from there.

The failure models differed significantly. For example, the ceramic capacitors had a long life but sudden cracking of the dielectric causes failure with a difficult-to-measure precursor event. The opto-isolator, by contrast, have a slow and measurable degradation over time due to damage to the lattice. This is shown in figure 4. Other devices such as the Power MOSFET's are in the middle but required a different type of test structure. In all cases of the critical components, it is necessary to establish an observation point for the individual components that reveals precursors, but does not itself contribute to failures.

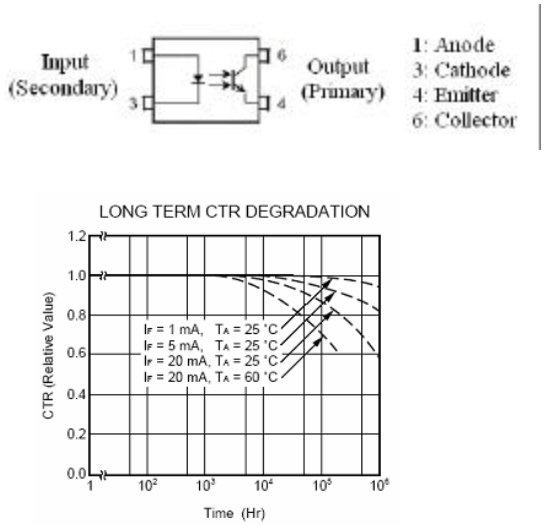


Figure 4. For the opto-isolator, there is a defined degradation in current transfer ratio (CTR) over time that leads to eventual failure. Other devices exhibit other kinds of degradation that can be measured as precursors to failure.

7. TEST POINT INSERTION (PROBES)

As a design objective, the prognostic sensor array was to be co-located with the host DC to DC Converter, with minimal impact to its performance, and operate in a "fail-safe" manner. The test points for this array are defined by access to the individual components that are to be observed. For this particular power supply, Ridgetop is able to observe the precursors using direct methods of measuring current or voltage.

To reach that objective, Ridgetop separated the test point sensor problem into three categories:

- In-situ observation of current or voltage is possible during normal operation.
- In-situ observation of current or voltage only possible if the component is disconnected from load (for example, as part of a power-up sequence)
- In-situ observation is not possible at all due to circuit topology considerations

The first two categories can be addressed through the use of a special current measurement hybrid design that attaches to key points within the circuit. This is shown in figure 5. The test points are selected through analysis of the Pareto Chart, which provides the ranking of most failure-prone devices. For optimum signal conditioning, there is some analysis required of the amplitude of the signals and the noise conditions present at the test point.

If no suitable means of direct observation is possible, as in the last category, then there is a fall-back to the statistical models that must be utilized.

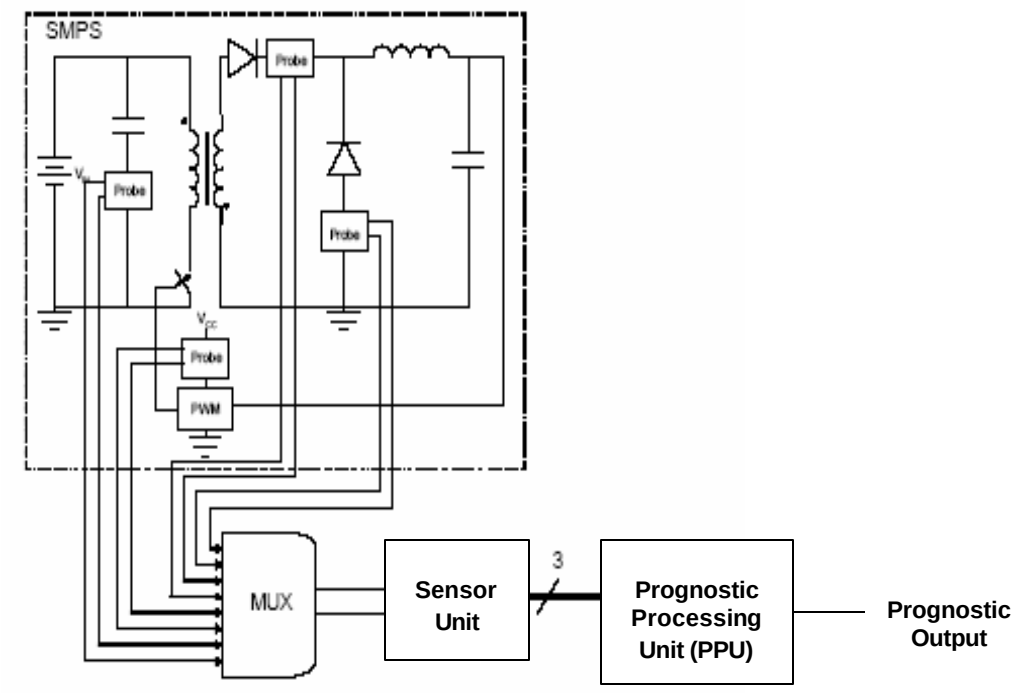


Figure 5. DC to DC Converter (simplified) with Probes and Sensor Unit

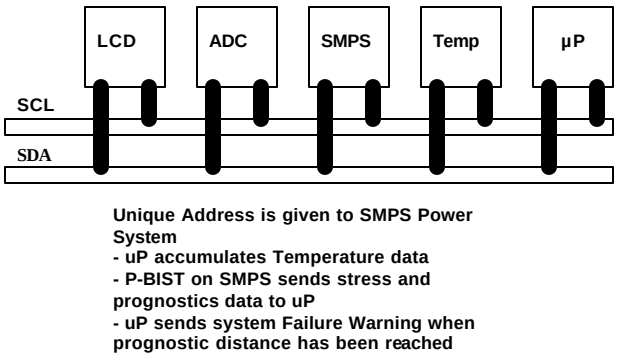
8. PROGNOSTIC PROCESSING UNIT (PPU)

After acquisition of the sensor array data, the data must be processed to yield a single "good' or "bad' indication, subject to user-supplied criteria. Ridgetop used a simple weighting algorithm for this purpose.

It is necessary to collect the distributed prognostic data from the SMPS, and develop a composite calculation on the health of the system based on this data. The calculation is initially simple; the components that have exceeded the prognostic distance are weighted by their importance (for example, bypass capacitors that fail open have a low weight, while Power MOSFETs have a larger weighting), and trigger an alert at the system level to take mitigating action to avoid a catastrophic failure. The calculation will be done by a uP located on the I^2C bus. (Figure 6)

Hardware Interface

The I^2C bus is a commercially-supported, 2-wire bus that is used by C & D Technologies (and others) in systems for power supply monitoring applications. The Master on the



bus always sends the clock signal and data is transmitted between master and slave at speeds of 100 KHz, 400 KHz or 3.4 MHz. One of the chief advantages
of this bus is that the devices that are attached to the bus are addressed completely by software and new functions can simply be clipped on the existing bus.

Figure 6. I^2C Bus Configuration with BIST/Prognostics from the SMPS

Using the 8051-type CPU operating as a Master on the bus, the overall stress factor can be calculated, by integrated voltage and temperature over time with the 8 bit processor provided by means of the I^2C bus. A composite BIST/Prognostics model can then be built and a means of transmitting the prognostic warning to the system.

Extensions to other Power System Implementations

The work described has been done using a simple forward switching converter, but the components in this converter are also present in other converter topologies, including a boost converter, sepic, cuk, resonant and other forms of high efficiency power conversion systems. Ridgetop will be extending its work into these other areas over time. Further areas of analysis also include noise tolerance to I^2C databus operation and optimizing the number of sensors and data transfer

9. SUMMARY

Ridgetop has completed the first phase of a multi-phase PHM implementation program on a high efficiency DC to DC converter. The results from this analysis indicate that certain failure rate components can be directly observed for precursors to failure. This will aid in providing a higher amount of operational readiness for the JSF Program.

Further work will be conducted by Ridgetop on larger sample sets under HALT Testing regimes at C & D Technologies.

The benefits to the Fleet in adding Electronics Prognostics/Health Management are as follows:

- Helps avoid catastrophic failures, preventing loss of life
- Addresses most troublesome and pervasive electronic subsystem – the power supply
- Increases the operational readiness for fleet assets
- Supports maintenance strategies tuned to operations and not strictly to elapsed time
- Provisioning and spares pipelines can be optimized with modules that have better lifetime estimates.
- Roots out the latent defects that otherwise escape detection.
- Augments information available through Built-in Test functions
- Redundancies may be reduced, with associated module weight, if the efficacy of Prognostics is established.

Transition plans to Navy Fleet

While the focus of this work is for the JSF, the potential applications for Electronic Prognostics are very large, and the solutions developed with this work will find wide applicability in other DoD System requirements. These include systems in aircraft, helicopters, ships and land-based systems. To the largest extent possible, Ridgetop has sought to make its Electronic Prognostics as modular as possible, so that the solution would (conceptually) snap-on with minimal rework of the host power conversion system.

Virtually all systems containing electronics have a power conversion system and this is the initial thrust of Ridgetop's prognostics innovations.

REFERENCES

[1] Goodman, Douglas L. "Prognostic Methodology for Deep Submicron Semiconductor Failure Modes", IEEE Transactions on Components and Packaging Technologies, Volume 24, Number 1, March 2001, pp. 109-111.

[2] Nigam, T. et al "A Fast and Simple Methodology for lifetime prediction of ultra-thin Oxides, 1999 IRPS Proceedings, pp 381-388

[3] Jones, M.R. "ACS WFC CCD Radiation Test – The Radiation Environment", Space Telescope Science Institute, May, 2000.

[4] "Power-supply reliability: a practical improvement guide", EDN, March 3, 1997 Karl H Pflueger, IBM Germany

[5] Eliasson, L. "Optimize Electrolytic Capacitor Selection", Power Electronics Technology, February, 2003

ACKNOWLEDGEMENTS

The authors would like to thank Andrew Hess and Tom Dabney from the JSF Program office for their support of this work under SBIR No. N68335-04-C-0088.

In addition, thanks go to Steve Wood and Don Gerstle of C & D Technologies and Jim Houston of Lockheed Martin Corporation for their support and encouragement.

BIOGRAPHIES

Doug Goodman *is the CEO of Ridgetop. He holds a BS in Electronic Engineering from California Polytechnic State University, San Luis Obispo, and has a Masters degree from the University of Portland. He has over 25 years of experience in low-noise instrumentation design, DFT and fault simulation techniques, and integrated circuit tool development. His previous affiliations include Tektronix, Honeywell and Analogy. He was on the patent committee at Tektronix, Inc. while in the firms' Laboratory Instrument Division. He has also served as an adjunct faculty member at the University of Arizona in Tucson.*

Dr. Bert Vermeire *is CTO at Ridgetop responsible for leading Research and Development Functions of the corporation. Bert has prior experience as Principal Investigator on several important projects dealing with advanced semiconductor processes, BIST Development and radiation hardening. Prior to the University of Arizona, Bert was with IMEC in Belgium. He received his PhD. from the University of Arizona, Tucson in 1999 and has written 27 technical papers.*

Phil Spuhler *received his B.S. degree in electrical engineering from the University of Arizona in May of 2003. Following his graduation he joined Ridgetop Group where he has worked on commercial product development in addition to completing design projects for NASA and Navy. His experience relating to prognostics consists of both board level and on chip prognostic designs and his main interests are in analog circuit design.*

Hari Venkatramani *is an Electronic Design Engineer at Ridgetop, and has previously worked on Ridgetop's earlier Prognostic Designs for DC to DC Converters. Hari received his BS in Electronic Engineering from Bombay University, India, and his MSEE from the University of Arizona. His thesis at the University of Arizona was in Prognostic Techniques for Semiconductor Failures.*