# Real-Time Detection of Solder-Joint Faults in Operational Field Programmable Gate Arrays

James P. Hofmeister
Ridgetop Group, Inc.
3580 West Ina Road
Tucson, AZ 85741
520-742-3300
hoffy@ridgetop-group.com

Pradeep Lall
Auburn University
Mech. Engineering and CAVE
Auburn, AL 36849
334-844-3424
lall@eng.auburn.edu

Edgar Ortiz
Douglas Goodman
Justin Judkins
Ridgetop Group, Inc.
3580 West Ina Road
Tucson, AZ 85741
520-742-3300
edgar@ridgetop-group.com
doug@ridgetop-group.com
justin@ridgetop-group.com

*Abstract*—In this paper we present two sensors for real-time detection of solder-joint faults in programmed, operational Field Programmable Gate Arrays (FPGAs), especially those FPGAs in Ball Grid Array (BGA) packages. The first sensor uses a method in-situ within the FPGA and the second sensor uses a method external to the FPGA. Initial testing indicates the first method is capable of detecting high-resistance faults of 100 Ω or lower and which last one-half a clock period or longer. A prototype of the second method detected high-resistance faults of at least 150 Ω that lasted as low as 25 ns. [1][2]

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## 1. INTRODUCTION

The authors present two sensors for real-time detection of solder-joint faults in programmed, operational Field Programmable Gate Arrays (FPGAs), especially those FPGAs in Ball Grid Array (BGA) packages, such as a XILINX® FG1156 [1]. FPGAs are used in all manner and kinds of control systems in aerospace applications. The ability to sense high-resistance faults in the solder joints of operational FPGAs increases both fault coverage and electronic Prognostics Health Management (ePHM) capabilities and support for condition-based and reliability-centered maintenance. As both the pitch between the solder balls of the solder joints of BGA packages and the diameter of the solder balls decrease, the importance of these sensors increases. The sensors presented in this paper are the first known for detecting high-resistance faults in solder joint networks of operational FPGAs.

These sensors are the first known for detecting high-resistance faults in operational I/O networks of programmed, operational FPGAs. Test assemblies of printed circuit boards (PWBs) with programmed FPGAs will be fabricated, populated and soldered for testing to failure. The completed boards will be tested at the Center for Advanced Vehicle Electronics (CAVE) at Auburn University during the Phase II period of a Small Business Innovation Research contract award; evaluation of one sensor, Sentinel Solder-Joint Built-in-Self-Test (Sentinel SJ BIST™) is being conducted at a German university under the sponsorship of an automobile manufacturer; and Raytheon Missile Systems is very interested in acquiring this technology.

The first sensor prototype, SJ BIST™, was realized as a two-pin test group core that was designed, programmed in a hardware description language, simulated, synthesized and loaded into an FPGA. SJ BIST correctly detects and reports instances of high-resistance and there are no false alarms: test results are shown in this paper. The test program, which contains temporary data collection routines for statistical analysis, uses less than 250 cells out of over 78,000 cells for a 5-million gate, 1156-pin FPGA to test 8 corner pins. Detailed designs for Highly Accelerated Life Test (HALT) experiments were completed at the time this paper was written: the design and layout of the PWBs is complete, and the Gerber files to manufacture those test boards have been produced.

The second sensor, Solder Joint Monitor (Sentinel SJ Monitor™), has been prototyped as a discrete component circuit for testing. In final form, SJ Monitor will be an Integrated Circuit (IC) chip. The prototype bread board version was built and tested to verify the sensitivity (detectable value of resistance) and the resolution (spike duration) of the second method. At the time of the writing of this paper, the design of the second type of sensor had been improved and a new prototype sensor was being built.

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[1] 1-4244-0525-4/07/$20.00 ©2007 IEEE.
[2] IEEEAC paper #1563, Version 2, Updated Dec. 14, 2006.

The sensor, a passive type of monitor, is expected to have improved resolution and sensitivity compared to the original design and implementation of SJ Monitor.

Initial testing indicates Sentinel SJ BIST is capable of detecting high-resistance faults of 100 Ω or lower and which last one-half a clock period or longer; SJ Monitor is capable of detecting high-resistance faults of 150 Ω or lower and which last for 50 nanoseconds or less. We are targeting the design point of SJ Monitor to be 100 Ω or lower with a fault duration of 25 nanoseconds or less. Our plans are to produce a final, commercialized version of SJ Monitor as an IC chip of less than 0.5 $mm^2$ for monitoring up to eight pins: the final package form has not been selected.

In addition to producing no false alarms in the current period of testing, we anticipate that neither SJ BIST nor SJ Monitor will introduce additional failure mechanisms to an assembly. This is because both SJ BIST and SJ Monitor, with the exception of fault reporting and handling, are (1) not invasive to an application program; (2) are not compute intensive and so timing problems are not anticipated; and (3) failures in SJ BIST and SJ Monitor are either going to result in no alarms or they will report alarms, which correctly indicate reduced reliability in the assembly.

*Mechanics of Failure*

Solder-joint fatigue damage is cumulative and is typically caused by thermo-mechanical and shock stresses. Fatigue damage manifests as voids and cracks, which propagate in number and size. Eventually, the solder joint fractures [2-5] and FGPA operational failures occur. An illustration of a damaged solder joint (or bump) on the verge of fracturing is shown in Figure 1.

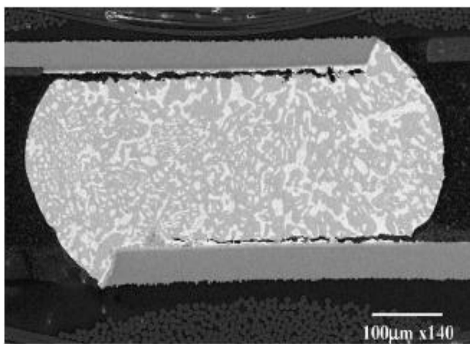


**Figure 1: Crack Propagation at the Top and Bottom of a Solder Joint, 15mm BGA [3].**

A significant cause of solder-joint fatigue damage is thermo-mechanical stress, especially in the horizontal direction as shown in Figure 2 because of the following [5-7]:

(1) Differences in coefficients of thermal expansion of the materials in the FPGA, the solder, the wiring, the interconnections and the printed wire board (PWB).

(2) Heating and cooling due to ambient temperature changes and to power-on and -off cycling. For example, grain boundaries in solder material continues to grow even when power is removed; increased grain boundaries lead to increased voids, which lead to increased onset of cracks.

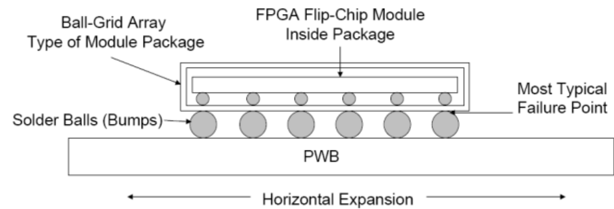


**Figure 2: FPGA Package, Solder Ball and Printed Wire Board Diagram Showing a Typical Failure Point.**

Fatigue damage can also accumulate because of stresses from shock, vibration and torque forces to which the assembled PWB is subjected to during missions, maintenance and storage. The accumulative damage eventually causes the solder joint to fracture, typically at the boundary of the solder ball and the package or at the boundary of the solder ball and the PWB, as seen in Figure 1 and Figure 2.

There are many possible points of failure in a solder-joint network. Referring to Figure 3, typical failure types and points are the following:

(1) Open in the wiring of the die between the buffers of an I/O port and the small solder bump.

(2) Open in the wire connection between the package and the die.

(3) Crack in the connection between the FPGA die and the outside of the chip module package.

(4) Crack through the solder bump.

(5) Crack between a solder bump and the wiring on a PWB.

The sensor methods presented in this paper are not sensitive or dependent upon a particular failure type or point of failure location.

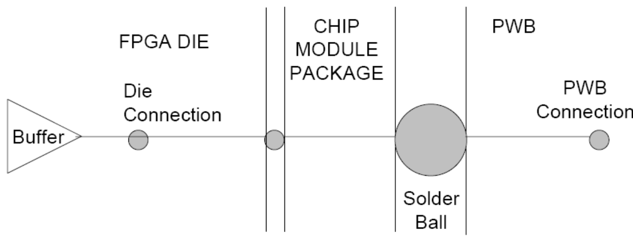


**Figure 3: Simplified Representation of a Solder-Joint Network.**

Subsequent mechanical vibration or shock tends to cause such fractured bumps to momentarily open and cause hard-to-diagnose faults of high resistance of hundreds of ohms or higher and lasting for periods of hundreds of nanoseconds, or less, to more than 1 µs [2, 5, 6, 8-11]. These intermittent faults in solder-joint networks increase in frequency as evidenced by a practice of logging BGA package failures only after multiple events of high-resistance: an initial event followed by some number (for example, 2 to 10) of additional events within a specified period of time, such as ten percent of the number of cycles of the initial event [9-11]. Even then, an intermittent fault of high-resistance in a solder-joint network might not result in an operational fault. For example, the high-resistance fault might happen in a single ground or power connection (where there are many other ground and power connections for the FPGA circuitry), or it might happen during a period when the network is not being written, or it might be too short in duration to cause a signal error. Figure 4 shows shock-actuated intermittent opens (high resistance).

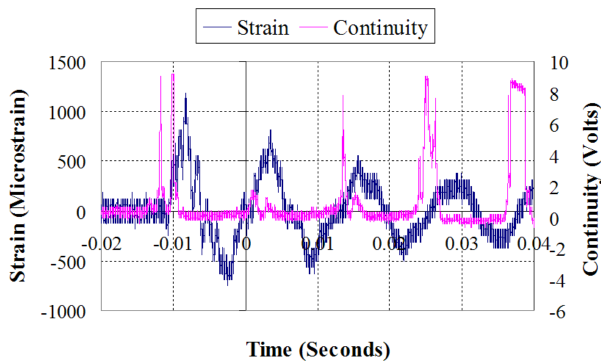


**Figure 4: Shock-Actuated Failure - Transient Strain and Resistance (from Lall).**

Figure 5 represents HALT test results performed on XILINX FG1156 Daisy Chain packages in which 30 out of 32 tested packages failed in a test period consisting of 3108 cycles. Each temperature cycle of the HALT was a transition from -55 °C to 125 °C in 30 minutes: 3-minute ramps and 12-minute dwells. What is not immediately apparent is that each of the logged FPGA failures (diamond symbols) represents at least 30 events of high resistance: a FAIL was defined as being at least 2 OPEN events (net resistance of 500 Ω or higher) within one temperature cycle, log 15 FAILURES [10]. A single OPEN fault in a temperature cycle was not counted as a FAIL event.

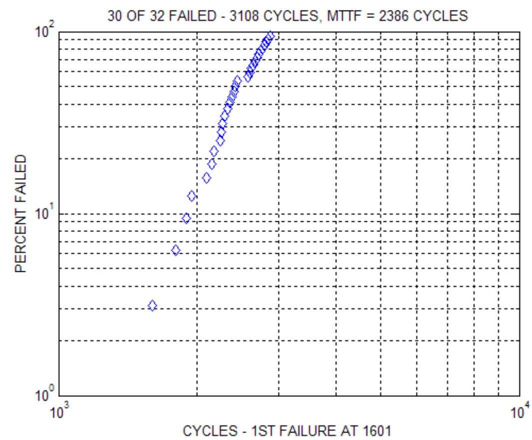


**Figure 5: Representation of XILINX FPGA HALT Test Results [10].**

*Location of Greatest Stress on FPGA I/O Ports*

The I/O pins, which are the solder balls, of an FPGA nearest the edges of the BGA package, especially those nearest to one of the four corners of a BGA package or die, experience the greatest thermo-mechanical stresses [12-15]. This is a good reason why the four solder joint locations at the corners of a XILINX FG1156 are connected to ground. This means that I/O pins on the outer edge of the BGA package that are near to one of the four corners are strong candidates for selection as SJ BIST test pins – those pins are likely to fail first.

*State of the Art*

In previous work, the authors have demonstrated the use of precursor indicators of failure for prognostication of electronics [12-15]. One important reason for using an SJ BIST or SJ Monitor type of sensor is stress magnitudes are hard to derive, much less keep track of, which leads to inaccurate life expectancy predictions [16]. Another reason for using SJ BIST or SJ Monitor is that even though a particular damaged solder-joint network (I/O port and the I/O pin circuit) might not result in immediate FPGA operational failure, the damage indicates the FPGA is likely to have other I/O pins that are damaged, which means the FPGA is no longer reliable. These sensors could also be used in newly designed manufacturing reliability tests to address a concern that failure modes caused by the PWB-FPGA assembly are not being detected during component qualification [7].

Modern FPGAs with millions of transistors are packaged as fine-pitch BGAs and ultra-pitch BGAs, such as the fine-pitch XILINX FG1156, and the packages have more than a

thousand I/O pins and very small pitch and ball sizes. The XILINX FG1156, packaged as fine-pitch BGA has a 34 x 34 array of nominal 0.60 mm solder balls with a pitch of 1.0 mm (see Figure 6). This tends to make physical inspection techniques impractical and not useful.

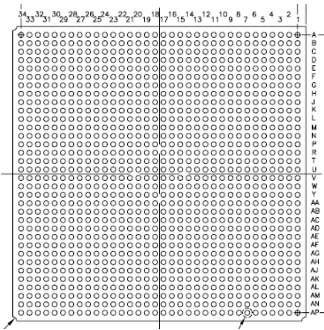

**Figure 6: Bottom View of a XILINX FG1156 – Package Size is 35 x 35 mm with a 34 x 34 Array of Solder Balls of Nominal Diameter of 0.6 mm and a Pitch of 1.0mm[1].**

Prior to these sensors, there were no known methods for detecting faults in operational, fully-programmed FPGAs. Furthermore, FPGAs are not amenable to the measurement techniques typically used in manufacturing reliability tests such as Highly Accelerated Life Tests (HALTs) [5]. This is because those measurement techniques require devices to be powered-off, and because FPGA I/O pins are connected to complex I/O port circuits, a representative I/O port circuit is shown in Figure 7. As seen in the figure, I/O ports contain tri-state buffers, diodes, resistors and logic input gates, which makes it difficult to detect damage to a solder-joint network, such as a high increase in resistance of the solder ball that attaches the FPGA I/O circuitry to the board.

## 2. REAL-TIME SOLDER JOINT SENSORS

This section presents two different methods for detecting high-resistance spikes: one is an in-situ sensor within the FPGA and is called SJ BIST; and the other is external to the FPGA and is called SJ Monitor.

*SJ BIST*

The innovative, in-situ SJ BIST method requires the attachment of a small capacitor to a test group of two non-flight functional I/O pins that are connected together. Preferably two unused I/O pins nearest a corner of the FPGA package are selected for testing as a two-pin group, and for good results, there should be one two-pin group for each corner. Figure 7 shows the I/O port circuitry for a single I/O pin for a XILINX FG1156.

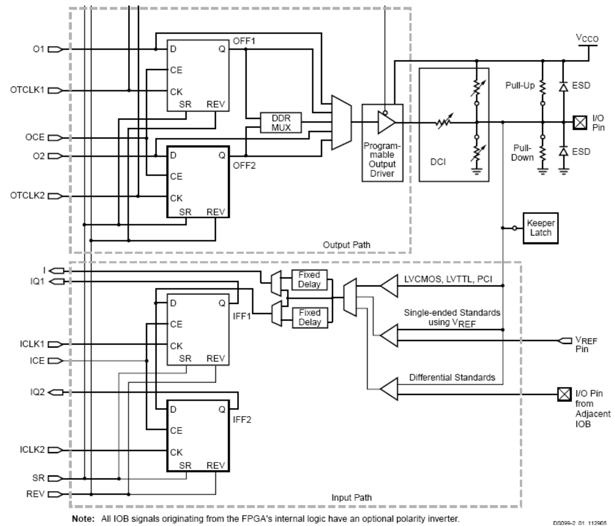


**Figure 7: Diagram Showing Input and Output Buffers - FG1156, XILINX Spartan Series [1].**

Figure 8 shows the block diagram of the SJ core (PC), inside of a FPGA on an application board.

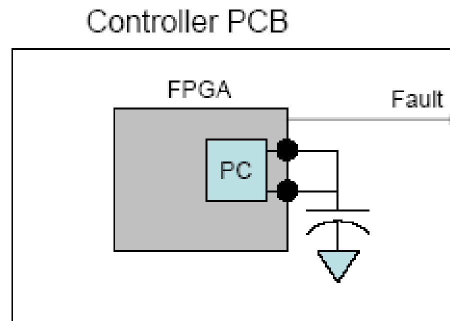


**Figure 8: Block Diagram, SJ BIST in Application FPGA.**

SJ BIST writes logical '1s' and '0s' to charge and discharge the capacitor and performs read checks. The occurrence of a high-resistance fault causes the capacitor to not fully charge, and a logical '0' instead of logical '1' is read by SJ BIST. A fault is detected and fault counts and signals are recorded for prognostic use.

*SJ BIST Test* – Figure 9 shows a test result: FPGA 10 MHz clock with no fault and with 100 Ω–fault injection on one of the I/O pins of a two-port test group. Various tests at 100 kHz, 1 MHz, 10 MHz, 20 MHz and 48 MHz were entirely successful: all instances of 100 Ω or higher faults were detected and reported with zero false alarms.

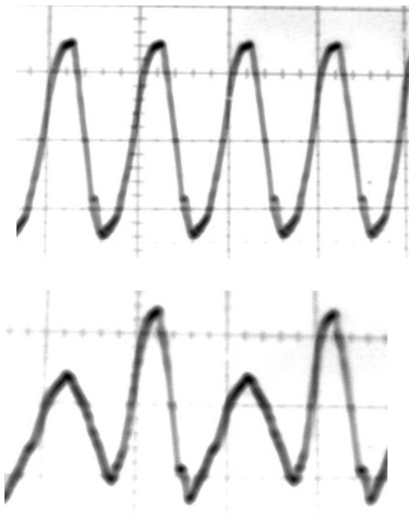

**Figure 9: SJ BIST Test, Two-Port Group; No-Fault Result on the Top, 100Ω-Fault Result on the Bottom; 10 MHz Clock, 1V-100nS Grid.**

*SJ BIST Plots* – Figure 10 is a family of curves that show the relationship of FPGA clock frequency, detectable resistance and external capacitor value.

As expected, as the clock frequency is increased, the value of the external capacitor needs to be reduced. The left-most plot in Figure 10 exhibits interaction between the parasitic (intrinsic) capacitance of the I/O port and the impedance, both resistive and capacitive, of the oscilloscope. With a clock frequency of 48 MHz, SJ BIST produced correct results simply by connecting the two I/O pins together – SJ BIST also produced correct results at that frequency with a very small, externally-attached capacitor.

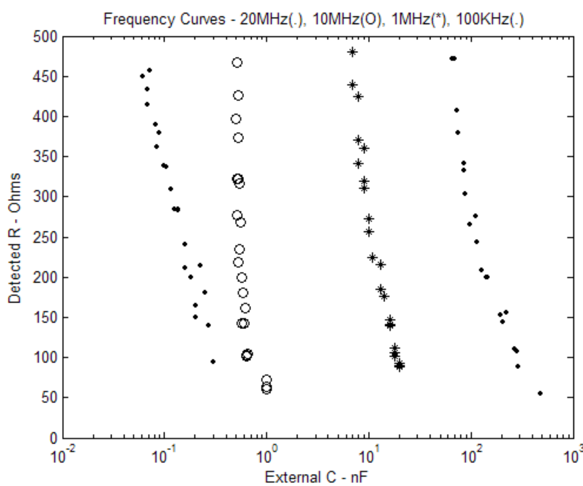


**Figure 10: Family of Curves Showing the R, C and the Clock Frequency Relationship.**

*SJ Monitor*

The innovative SJ Monitor method physically differs from the SJ BIST in the following manner: (1) it is external to the FPGA rather then internal; (2) it does not require an external capacitor, and (3) a single I/O pin is tested by each SJ Monitor.

Figure 11 shows a high-level block diagram that shows a prototype SJ Monitor cell attached to a single I/O pin of an application FPGA on an application board. The final version of SJ Monitor is to be an IC chip that can be mounted on the PWB assembly to be tested or mounted on a separate monitoring assembly.

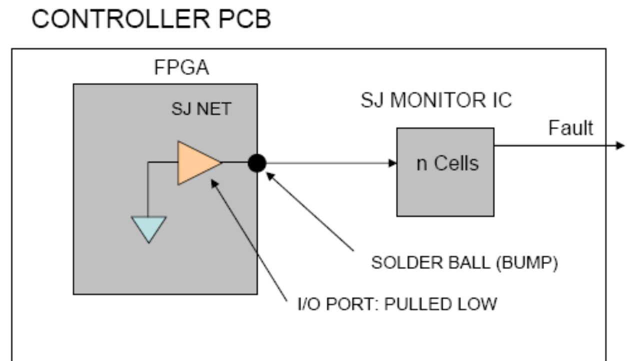


**Figure 11: Block Diagram, Prototype SJ Monitor on Application Controller Board.**

*SJ Monitor Test* – Figure 12 shows a test result for SJ Monitor with an injected fault of 150 Ω, 50 ns.

**Figure 12: SJ Monitor Test: 150Ω Fault Causes an I/O Pin Pertubation (Top) That is Detected (Bottom); Fault Duration Was About 50ns - X-axis is 50ns and Y-axis is 100mV.**

Following the successful test of the initial prototype SJ Monitor, the design was modified and a second prototype SJ Monitor is being built in anticipation of increasing the sensitivity to detect fault resistance of 100 Ω or less and increasing the resolution to detect faults lasting 20 ns or less.

## 3. SJ BIST AND SJ MONITOR

*Signals and Controls*

SJ BIST, at minimum, must present at least one error signal (a fault indicator) either to an external FPGA I/O port or to an internal fault management program. For evaluation and investigation, the prototype SJ BIST core provides two fault signals plus fault counts. Similarly, SJ Monitor provides two fault signals plus fault counts.

Both SJ BIST and SJ Monitor accept controls signals to enable, to disable and to reset the test, the signals and the counts.

*Error Signal and Count* – The prototypes produce two fault signals as follows for each tested I/O pin: (1) at least one fault has been detected, and (2) a fault is currently active. For a multiple-pin test, these signals can be ORed together. The prototypes also produce a count of the number of detected faults for each tested I/O pin: 8-bit, 255-count.

For a deployed SJ BIST, we anticipate most applications would only use the two error signals. We also believe a deployed SJ BIST application would most likely use at least four cores of 2-pin groups – one core for each corner of an FPGA.

*Controls* – In addition to CLK, SJ BIST has two input-control signals: ENABLE and RESET. ENABLE is used to turn SJ BIST detection on and off; RESET is used to reset both the fault signal latches and the fault counters. For a deployed SJ BIST, RESET might not be used.

SJ Monitor does not use a clock, only ENABLE and RESET, both of which operate the same as for SJ BIST.

*SJ BIST and SJ Monitor Advantages and Disadvantages*

Our current effort is focused on the design and development of two SJ BIST cores: (1) a two-port, two-pin-test core; and (2) a two-port, one-pin-test core. To test more than one or two I/O pins, we believe that multiple SJ BIST cores should be used in the deployed FPGA.

Each of the SJ BIST core designs has disadvantages and advantages:

(1) For "guaranteed" detection of a fault, a two-port, two-pin-test SJ BIST requires two clock cycles to test both pins compared to one clock cycle for a two-port, one-pin-test SJ BIST. Both methods are capable of detecting faults that less for less than one-half of clock period, but only if the fault occurs at the beginning of write for that I/O pin.

(2) To test 8 I/O pins, the two-port, two-pin-test core requires 4 external capacitors. A two-port, one-pin-test core requires 8 instead of 4 external capacitors and requires, in comparison, more power to run the test.

(3) In comparison to SJ BIST, SJ Monitor uses more I/O ports and more combinatorial logic to test, for example, the 8 I/O pins nearest the four corners of an FPGA package.

*SJ BIST and SJ Monitor Comparison*

The following is a list of comparisons of between SJ BIST and SJ Monitor:

(1) The logic for SJ BIST preferably resides in the FPGA to be tested; the implementation of the SJ Monitor is external to an FPGA.

(2) SJ BIST requires external capacitors to be attached to FPGA I/O pins; SJ Monitor attaches to FPGA I/O pins.

(3) SJ BIST uses more power compared to SJ Monitor.

(4) SJ Monitor, even in the form of an IC chip, occupies more real-estate on a board compared to SJ BIST.

## 4. CONCLUSION AND SUMMARY

In this paper we presented an overview of the physics of failure associated with the solder joints of FPGAs in BGA packages: the primary contributor to fatigue damage is thermo-mechanical stresses related to CTE mismatches, shock and vibration, and power on-off sequencing. Solder-joint fatigue damage can result in fractures that cause intermittent instances of high-resistance spikes that are hard-to-diagnose. In reliability testing, OPENs (faults) are often characterized by spikes of a couple of hundred ohms or higher that last for 200ns to 1μs or longer.

SJ BIST uses a method wth programmed cors in-situ within the FPGA plus a small capacitor attached to each two-pin test group; SJ Monitor uses a method external to the FPGA and in final form will be packaged as an IC chip. Initial testing indicates SJ BIST is capable of detecting high-resistance faults of 100 Ω or lower and which last one-half a clock period or longer. The first prototype of SJ Monitor detected high-resistance faults of 150 Ω lasting for 50 ns. A new design is being prototyped that is expected to increase the sensitivity to about 100 Ω and the resolution to about 20 ns.

Prior to SJ BIST and SJ Monitor, there were no known methods for detecting high-resistance faults in solder-joint networks belonging to operational, fully-programmed FPGAs.

SJ BIST and SJ Monitor used to test and monitor operational FPGAs are important addition to prognostic

health and management because stress magnitudes are hard to derive, which leads to inaccurate life expectancy predictions; and even though a particular damaged solder-joint port might not result in immediate FPGA operational failure, the damage indicates the FPGA is no longer reliable. An in-situ SJ BIST can also be used in newly designed manufacturing reliability tests to investigate failure modes related to the PWB-FPGA assembly.

We believe that without SJ BIST and SJ Monitor, there is a serious lack of capability given the current direction and progress in designing and implementing an electronic prognostic schema. Additionally, SJ BIST and SJ Monitor will prove to be extremely valuable for implementing digital electronic PHM.

Two prototype SJ BIST cores and one SJ Monitor prototype circuit have been designed. The two-port SJ BIST was programmed, simulated, synthesized, loaded into a FPGA on a development board and tested in a laboratory. The test results show the SJ BIST core correctly detects and reports instances of high-resistance without false errors – no errors detected or reported when the network resistance is 1.0 Ω or less.

The fault signals and counts provided by both SJ BIST and SJ Monitor are exploitable for ePHM purposes. We have identified a useable fault-to-failure signature that can be modeled and used to produce Remaining Useful Life estimations.

SJ BIST and SJ Monitor could be used to increase manufacturing reliability by using them to verify the robustness and reliability of assembled boards. Faults occurring within a small number of cycles of a Highly Accelerated Screen Test indicate premature failure of the solder joints. The value of increased reliability in aerospace applications versus cost is difficult, if not impossible, to measure, especially when the cost of SJ BIST and SJ Monitor per FPGA is likely to be in range of dollars or less (we are still in the design, evaluation and testing phases and have not determined or set commercial prices).

## 5. Future Activities

Extensive HALT experiments will be run. Some of the desired results of those experiments are the following:

(1) Determination of the minimum detectable fault duration.

(2) The minimum sensitivity of SJ BIST and SJ Monitor.

(3) The minimum resolution of SJ BIST and SJ Monitor.

(4) The optimal capacitor size to use for a range of clock frequencies.

(5) Statistical measures related to test I/O pin location and first failure.

(6) Reliability measurements and statistics.

Continue working on design improvements, especially for SJ Monitor. Our goal is for a minimum sensitivity of 100Ω and a minimum resolution of 1 clock cycle for SJ BIST and 20 ns for SJ Monitor.

The project includes provision for producing a SJ Monitor transistor-level of design, the integrated circuit (IC) masks for that design, and fabrication and test of SJ Monitor as IC chips.

## Acknowledgement and Patents

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Two final patent applications were filed in January and February of 2006: both for the innovations presented in this paper [17]. Both applications were published by the U.S. Patent Office in August of 2006.

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## BIOGRAPHY

***James Hofmeister*** *is a senior principal engineer and principal investigator. He has been a software architect, designer and developer for IBM, a software architect, electronic design engineer, principal investigator on research topics and co-inventor of electronic prognostics at Ridgetop Group. He is a former director, representing IBM, of the Southern Arizona Center for Software Excellence, a co-author on five IBM patents, and a co-author on four pending Ridgetop patents, two of the four have been published by the U.S. patent office. He retired from IBM after a 30-year career and joined Ridgetop Group in 2003. He received a BS in electrical engineering from the University of Hawai'i, Manoa Campus, and a MS in electrical and computer engineering from the University of Arizona.*

***Pradeep Lall*** *is the Thomas Walter Professor, Department of Mechanical Engineering and Associate Director of NSF Center for Advanced Vehicle Electronics at Auburn University. Dr. Lall has ten years of industry experience and has published extensively in the area of electronic packaging with emphasis on modeling and predictive techniques. He holds several U.S. patents, and he is an Associate Editor for the ASME Journal of Electronic Packaging, IEEE transactions on Components and Packaging Technologies and IEEE Transactions on Electronic Packaging Manufacturing. He received the MS and Ph.D. degrees from the University of Maryland and the M.B.A. from Kellogg School of Management.*

***Edgar Ortiz*** *is an electronic design engineer for electronic prognostics at Ridgetop Group in Tucson, AZ. He received a BS in computer engineering from the University of Arizona with minors in computer science, electrical engineering and mathematics. He is currently involved in the testing and design of projects at Ridgetop Group dealing with a wide range of topics such FPGAs, solder joint, digital-to-analog converters and field effect transistors.*

***Doug Goodman*** *is President and CEO and has 30 years of design and development experience. He has been a principal investigator on research topics and is a co-author on a pending Ridgetop Group patent. He was a co-founder of Opmaxx, which was acquired by Credence in 1999; prior to that, he was VP of Engineering for Analogy, which is now part of Synopsys; and he held responsible positions at Textronix, Inc. He received a BS in electrical engineering from California Polytechnic State University and an MBA from the University of Portland, Oregon.*

***Justin Judkins*** *is Director of Research and oversees the research and implementations of electronic prognostics. His research interests involve applying sensor array technology to various reasoning engines to provide optimum performance for electronic modules and systems. He is a co-author on two pending Ridgetop Group patents. He previously held senior-level engineering positions at Bell Labs and Lucent involving high-reliability telecom transmission. He received his Ph.D. in electrical engineering from the University of Arizona.*