Testing and Design-for-Testability Solutions for 3D ICs

The Hype, Myths, and Realities

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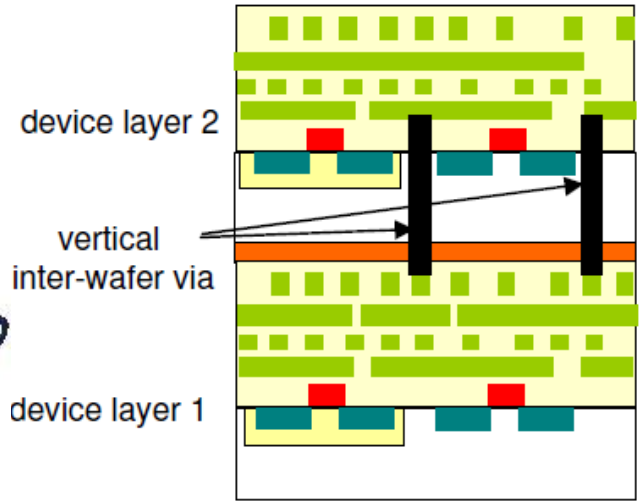

DUKE
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Outline

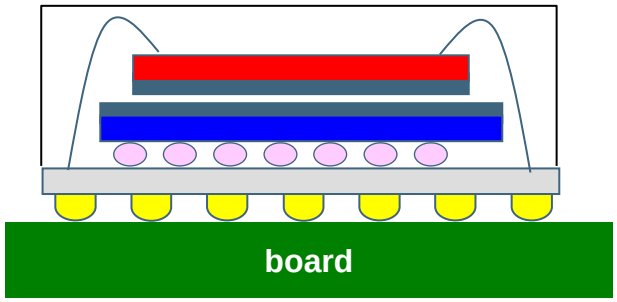
- Technology Overview
- Hype, Myths, and Reality
- 3D IC Test Challenges
  - What to test? When to test? How to test?

- *Emerging* Solutions
  - Recent advances
  - Some controversies

Stacking with Through-Silicon Vias (TSVs)

Traditional stacking with:

3D chip stacking with wire-bonds:
Heterogeneous technologies
Not-so-dense integration, Not-so-small footprint

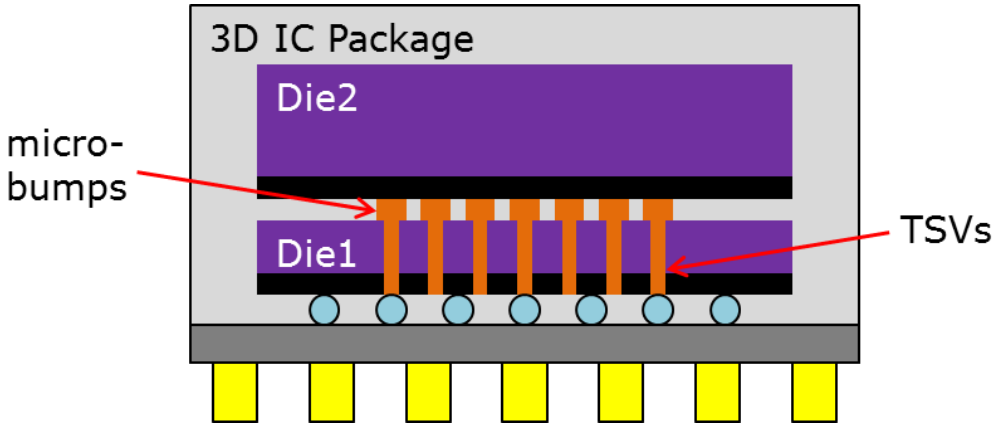


System-in-Package (SiP)

New stacking technology:

Through-Silicon Vias (TSVs):
Metal vias that provide interconnects from front-side to back-side through silicon substrate

Diameter	5 µm
Height	50 µm
Aspect ratio	10:1
Minimum pitch	10 µm

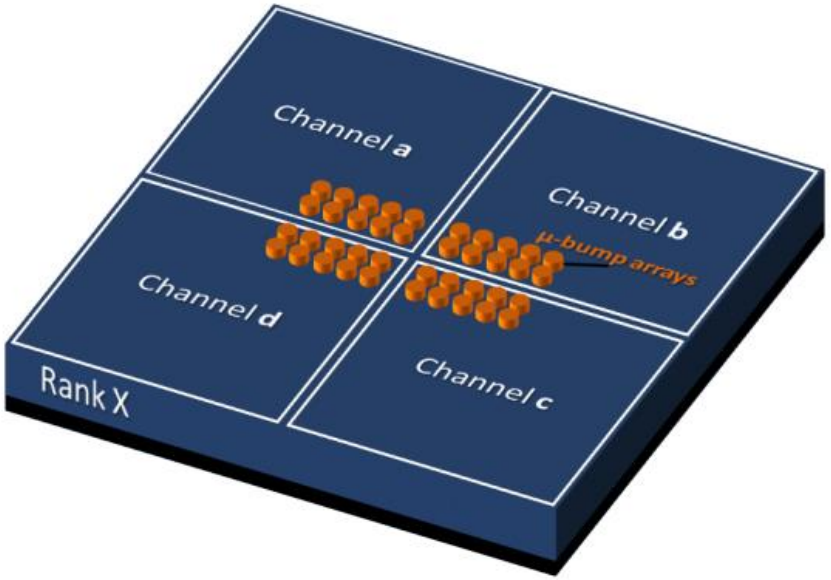


TSV-Based 3D-SIC

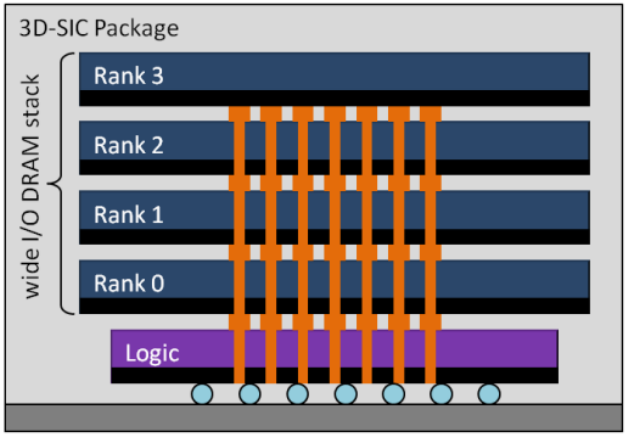
Applications

Memory-on-Logic (JEDEC Wide I/O DRAM)

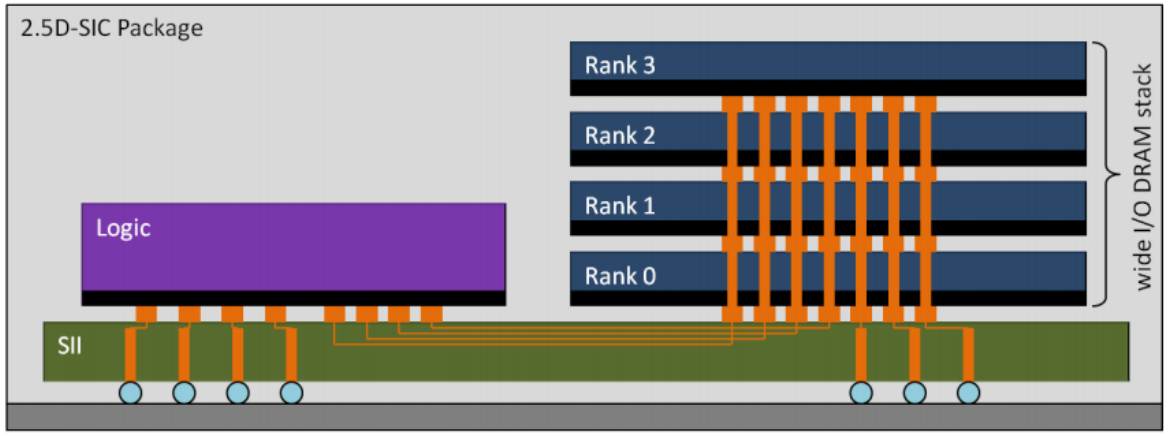
- 4 channels (*a*-*c*)
- 4 x 128 bit = 512 bit I/O
- 4 x 4.25 Gbytes/s = 17 Gbytes/s bandwidth
- Up to 4 stacked dies (Rank 0-3)



3D-SIC



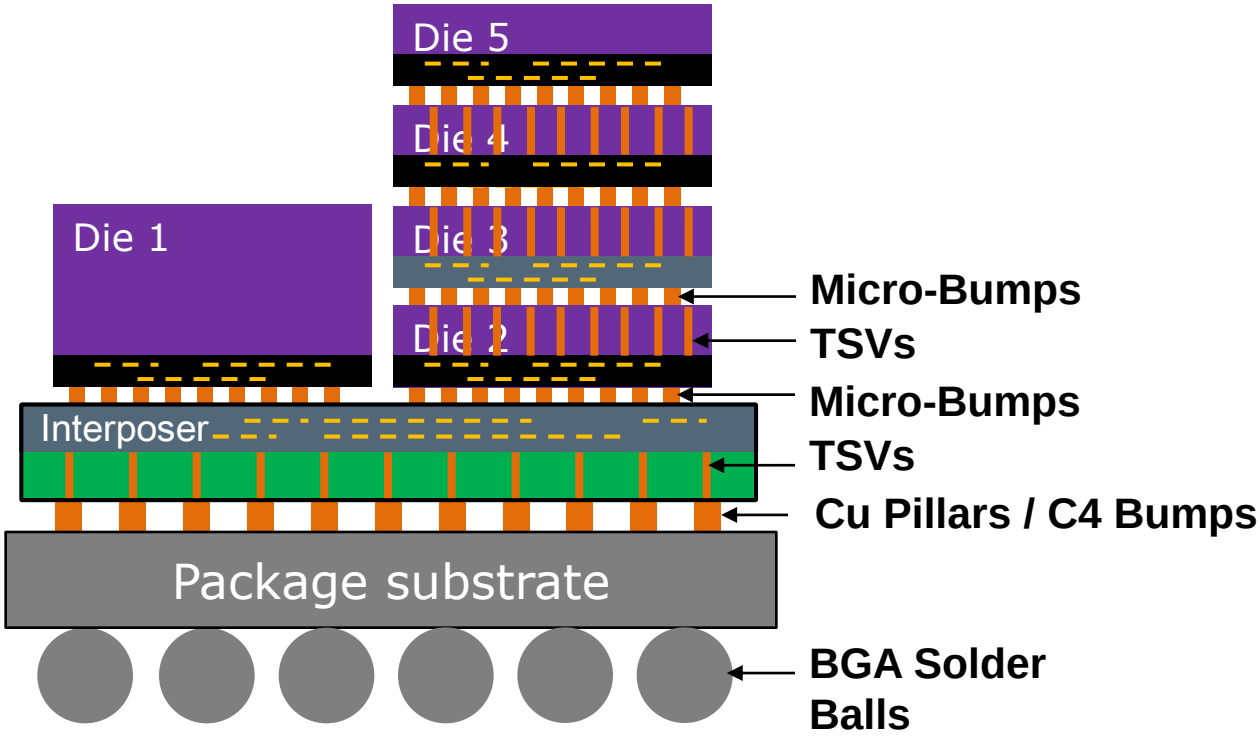
2.5D-SIC



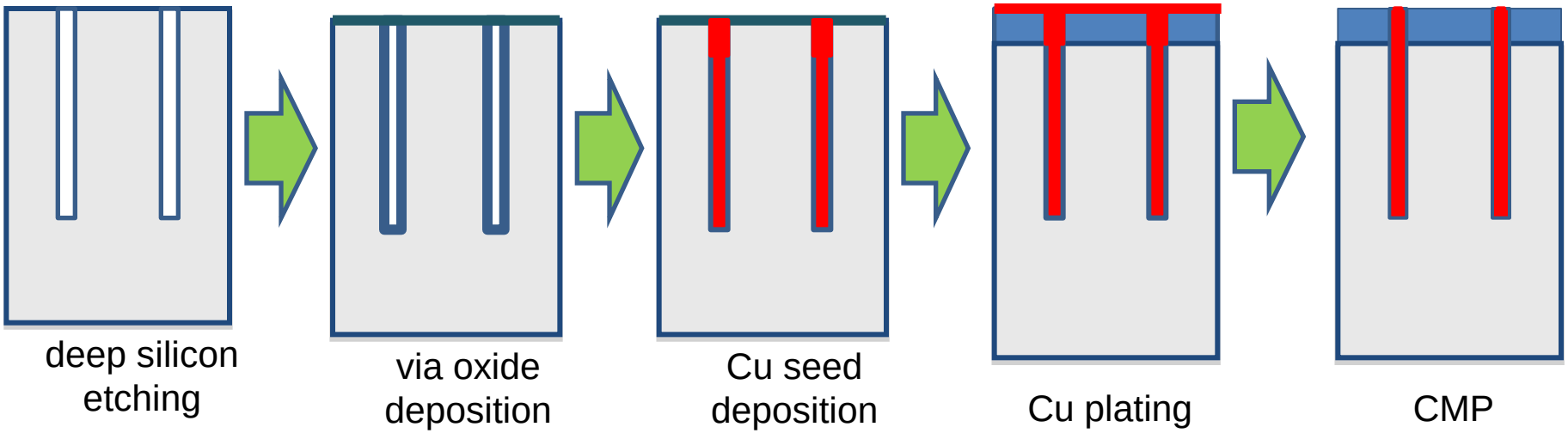
Applications

Future applications:

- Logic-on-logic
- Multi-tower stacks (both logic-on-logic and memory-on-logic)



TSV Formation, Wafer Thinning



Difficult to process wafers thinned below 100 microns

- Mount wafers on temporary wafer handlers (carriers)
- Thinning and backside processing

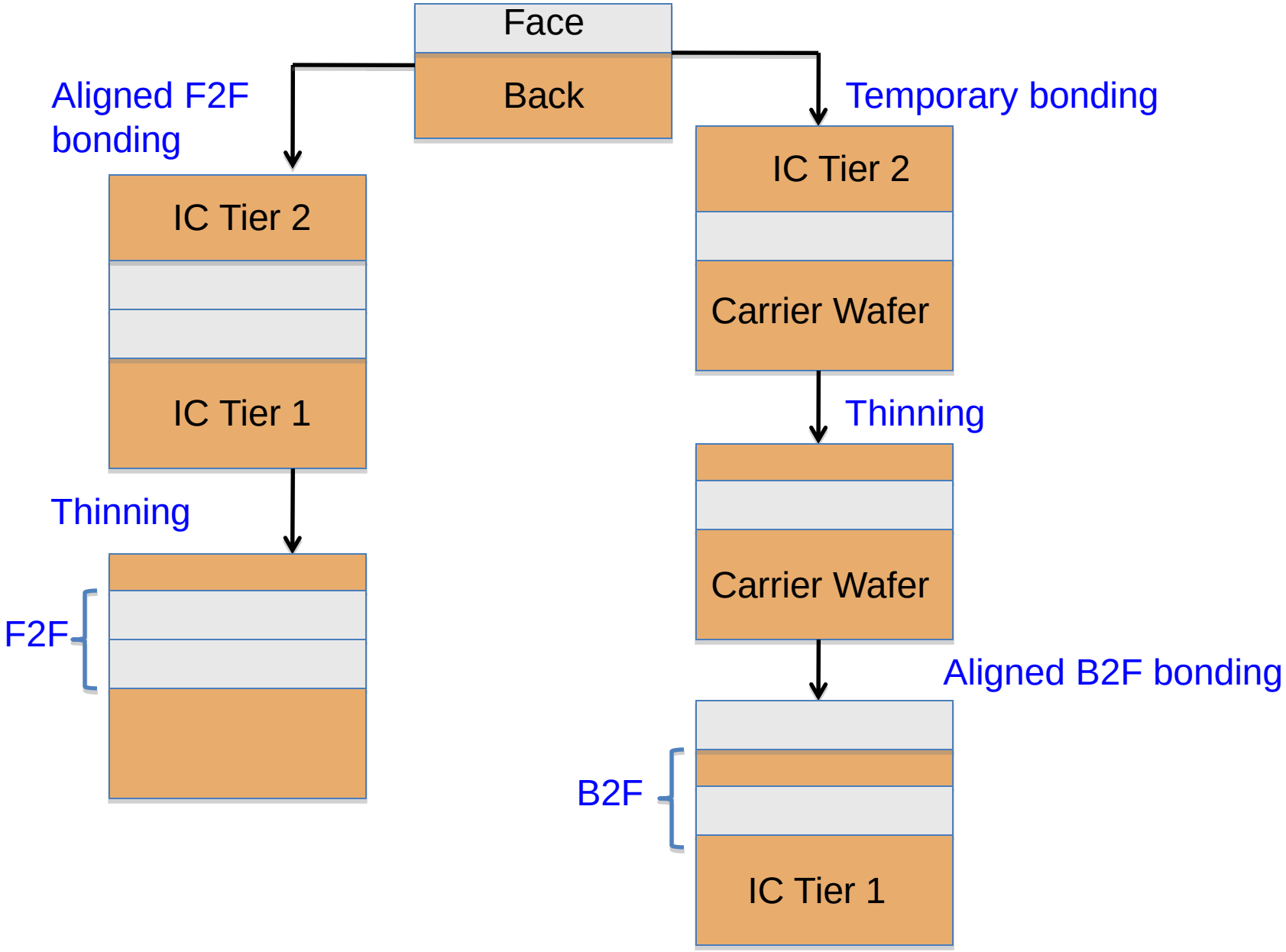
Option 1: Mount IC wafer face-down on carrier, bond “face-up” (B2F)

- Scalable solution, supports more stacked layers

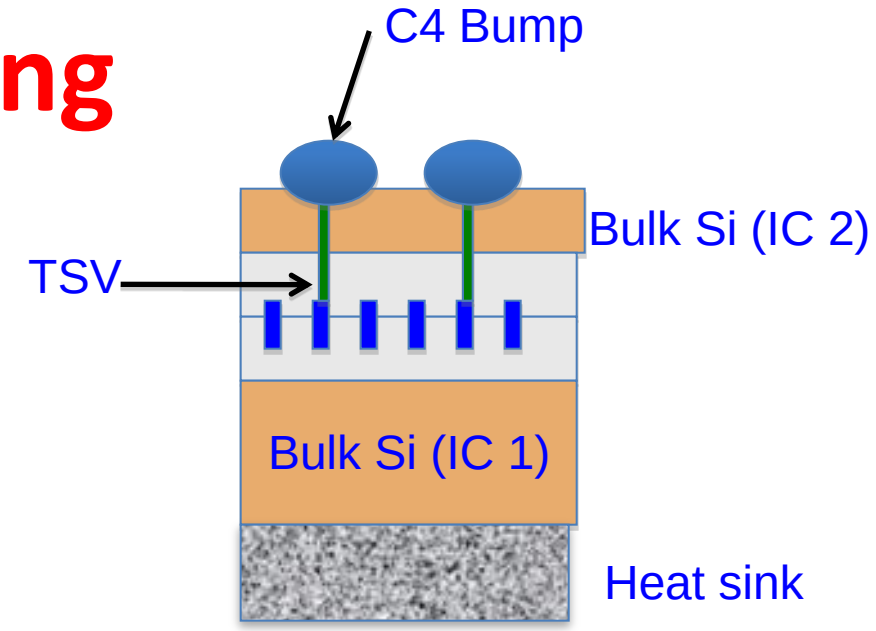
Option 2: Bond wafer to 3D stack in “face-down” configuration (F2F)

- More interconnects between active device on two layers
- Number of stacked dies limited to 2

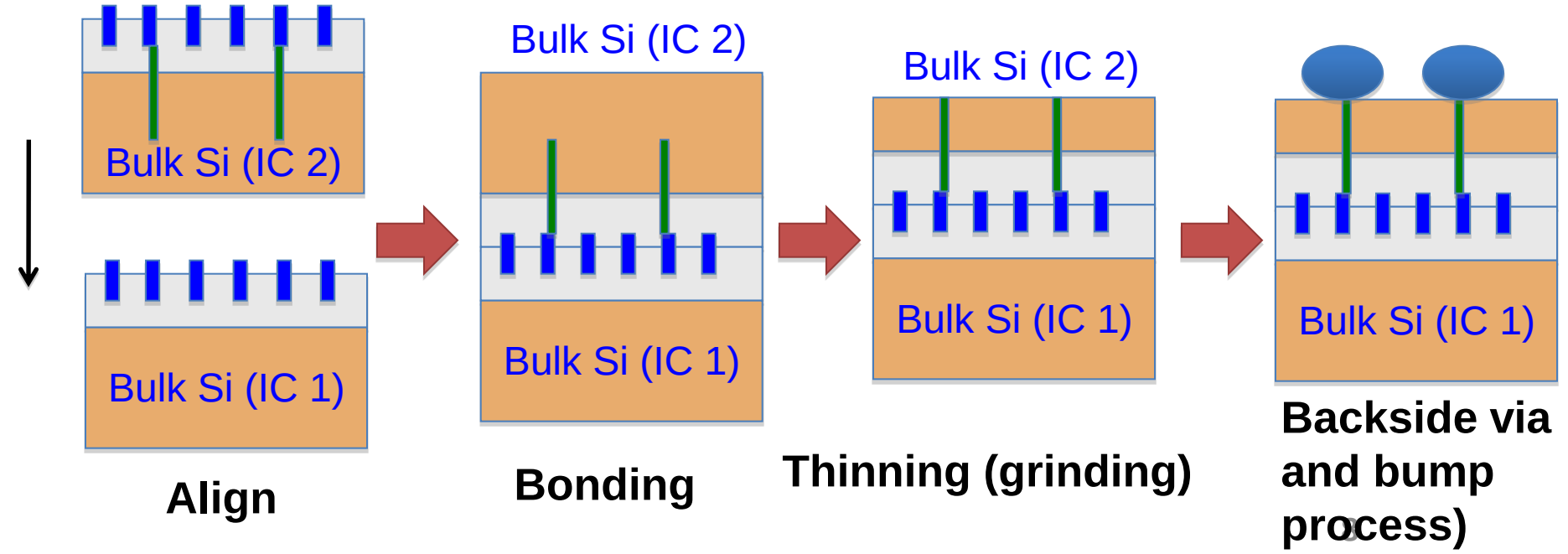
Fabrication of IC Stacks



Steps in F2F Bonding

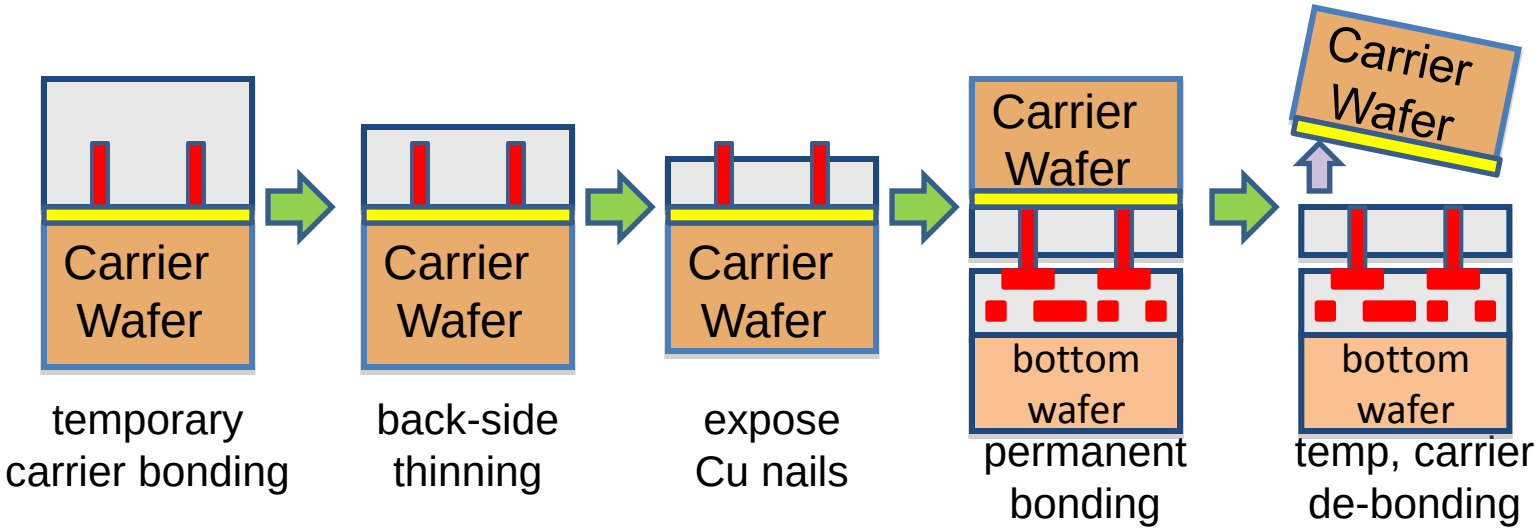


TSV prefabricated, but buried



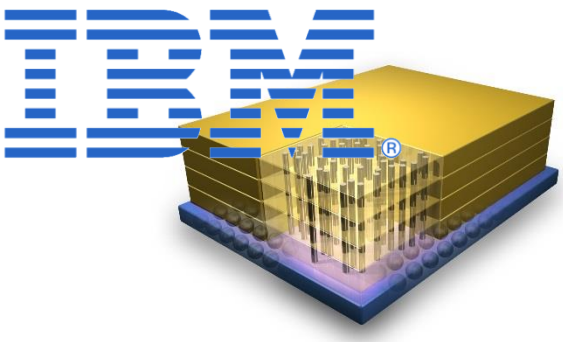
Align **Bonding** **Thinning (grinding)** **Backside via and bump process)**

Steps in B2F Bonding



Hype: Industry Trends in 3D Integration

3D-IC Reference Flow: CoWoS



TSV process for narrow pitch: 10µm

GLOBAL FOUNDRIES

20nm technology with TSVs

NVIDIA

About to stack DRAM on Volta GPUs

imec

Research in 10µm-pitch micro-bumps

amkor

€25M investment for in-house production of 3D ICs

Hype: Industry Trends in 3D Integration

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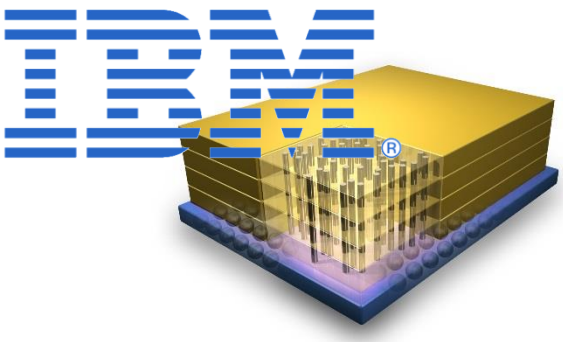

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amkor

€25M investment for in-house production of 3D ICs

Hype: EDA Support for 3D Flows

cadence™

- Tools for 3D included in TSMC Reference Flow
- Validated on a memory-on-logic design with Wide-I/O DRAM

Mentor Graphics®

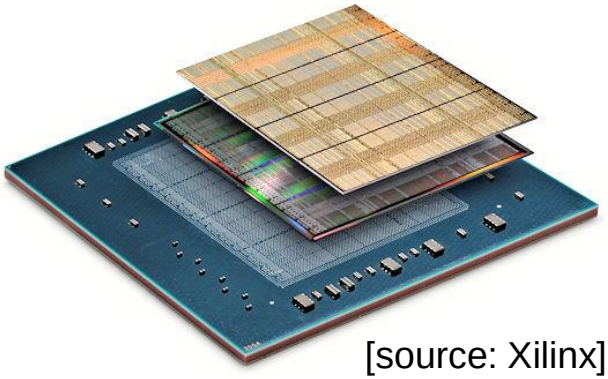
- Tools for 3D included in TSMC Reference Flow

SYNOPSYS®

- Collaborates with A*STAR IME to Optimize Through-Silicon-Interposer (TSI) Technology

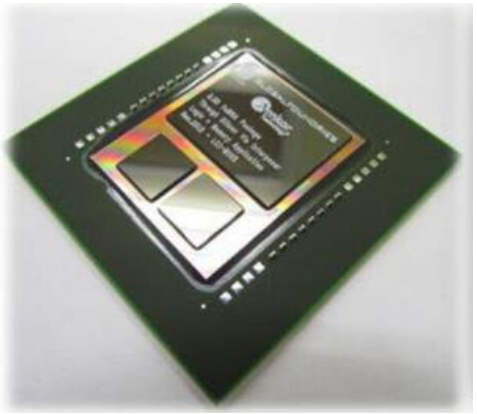
3D ICs: Reality

- 3D stacking technology demonstrated on silicon (but limited)
  - Xilinx, TSMC, GlobalFoundries, AMD



[source: Xilinx]

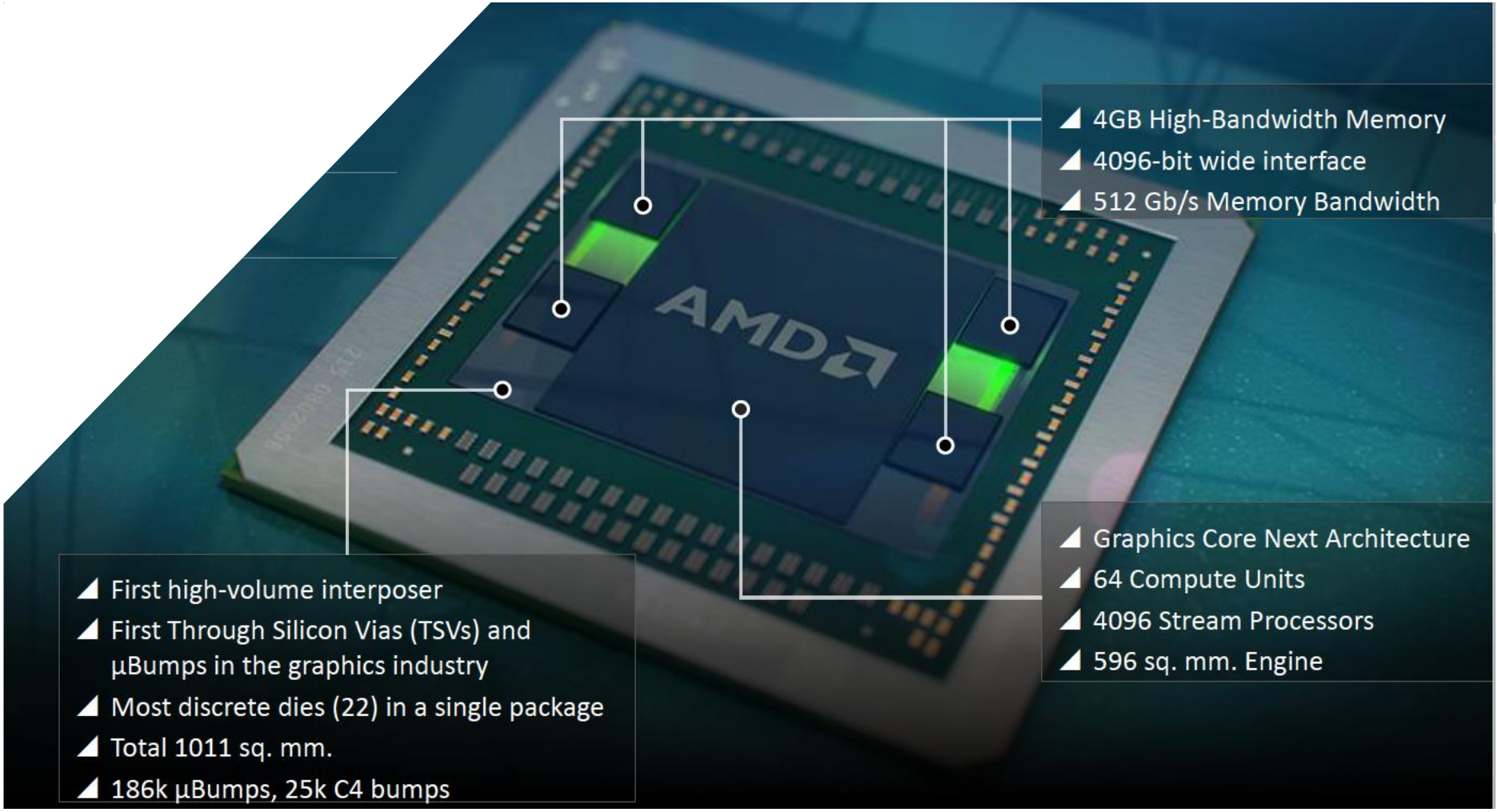
[source: TSMC]



[source: Globalfoundries]

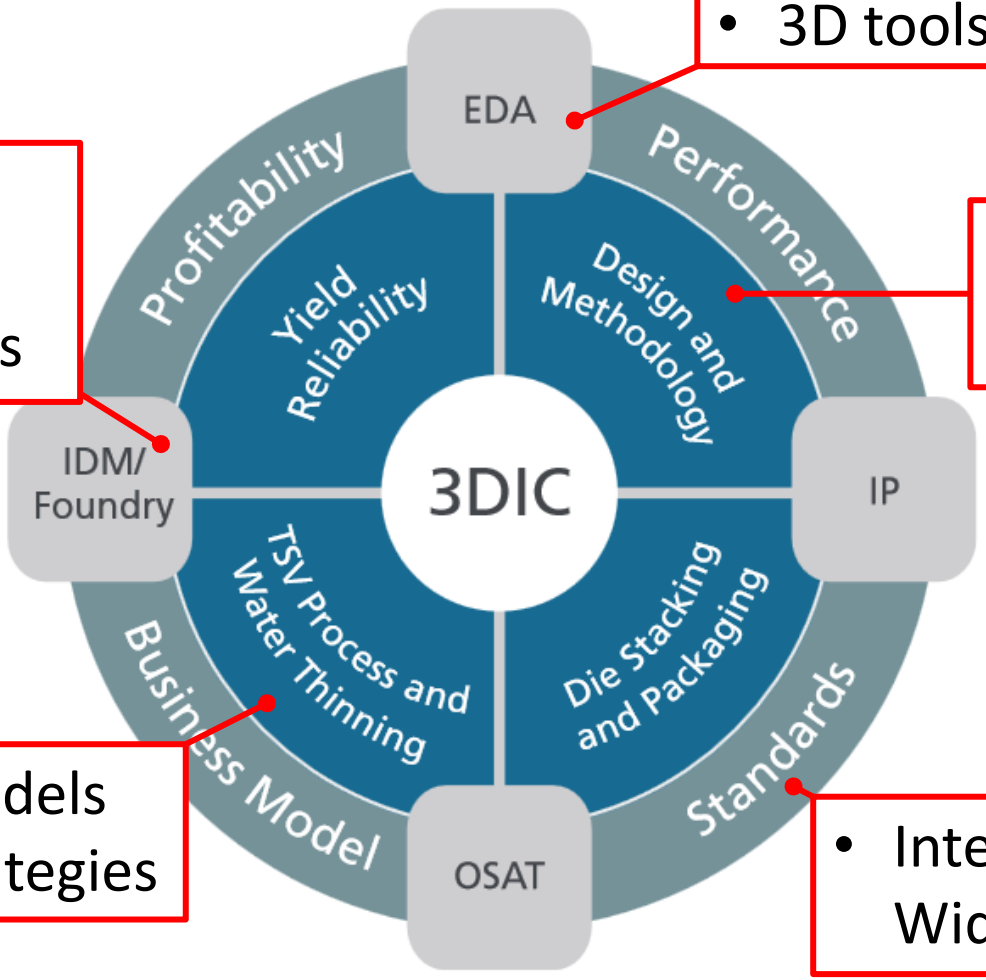
- Cost remains ultimate challenge
- Efficient 3D IC ecosystem needed for high-volume manufacturing

3D ICs: Reality (AMD “Fiji”)



Jeff Rearick, 3D Test Workshop, 2015

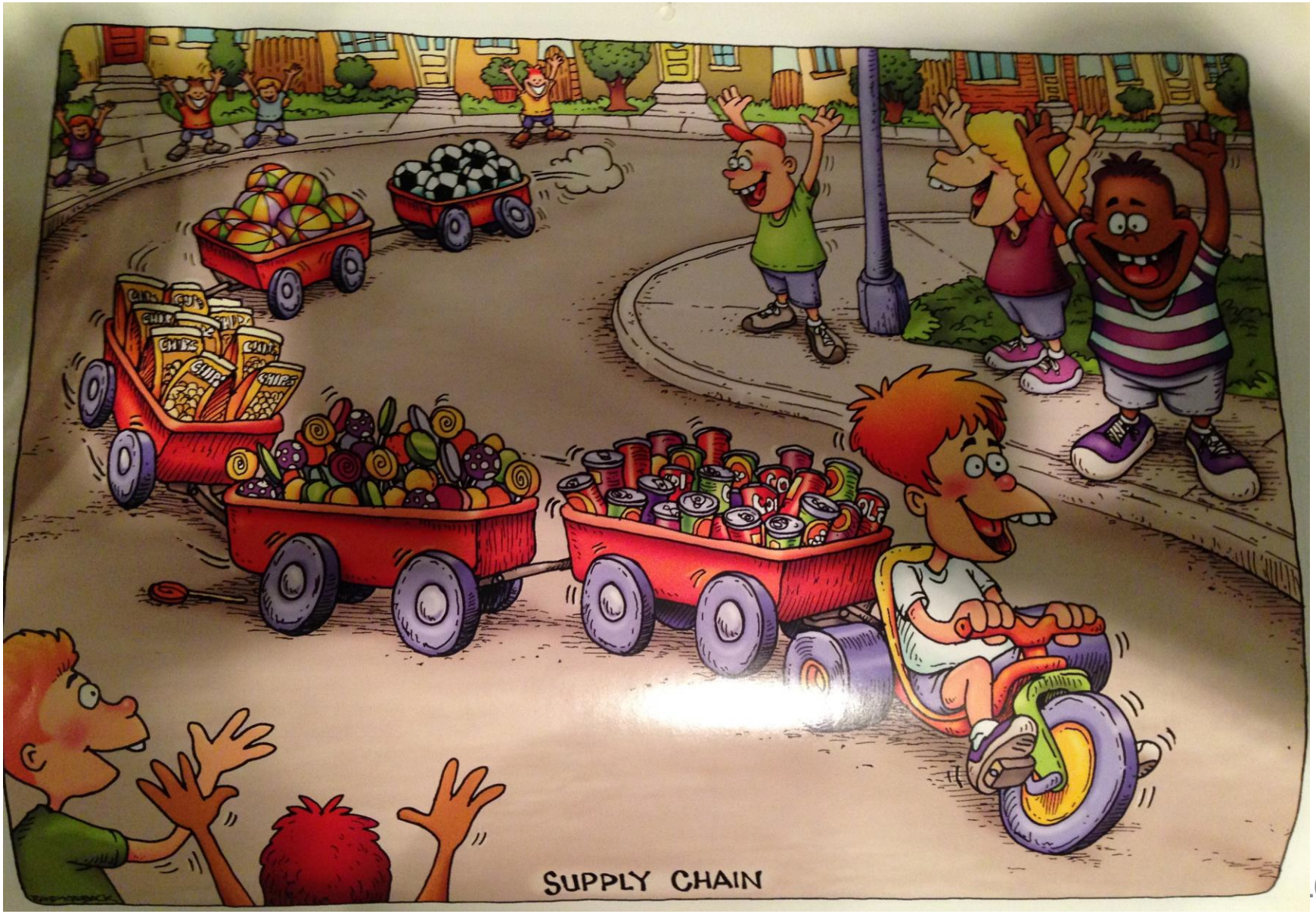
Reality: Need for 3D IC Ecosystem



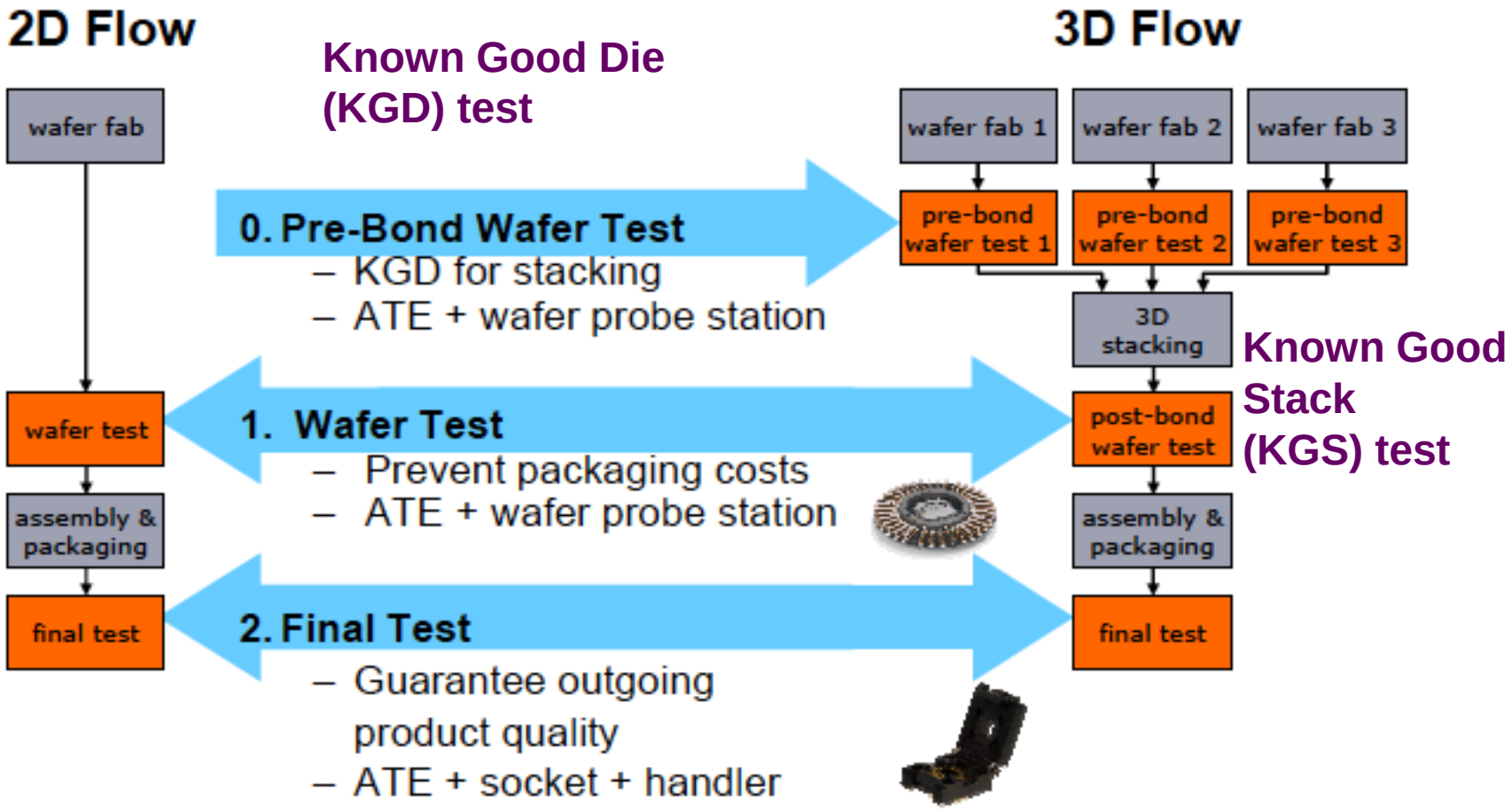
- 3D tools
- Libraries
- PDKs
- Ref. flows
- 3D partitioning
- Floor planning
- Cost models
- Test strategies
- Interface standards: Wide I/O, test I/O

[source: cadence.com]

Reality: Supply Chain Needed



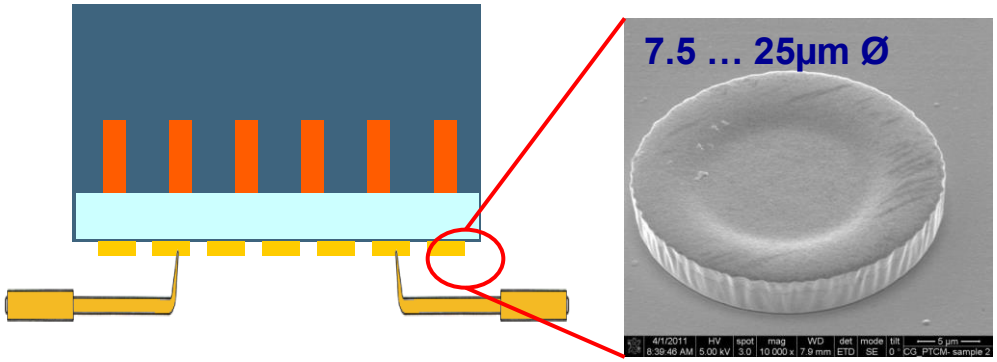
From Two to Three (or More?) Test Insertions



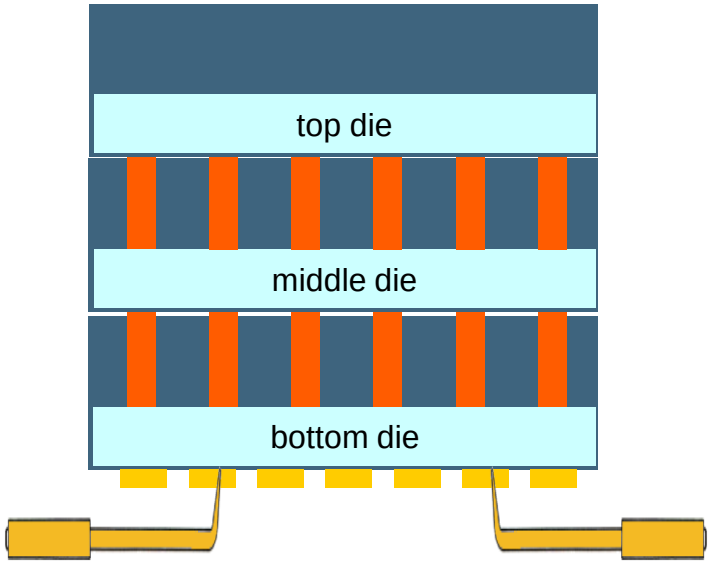
Test Content, Test Delivery, Test Resource Optimization and Reuse (Cost Minimization)

3D Test Challenges

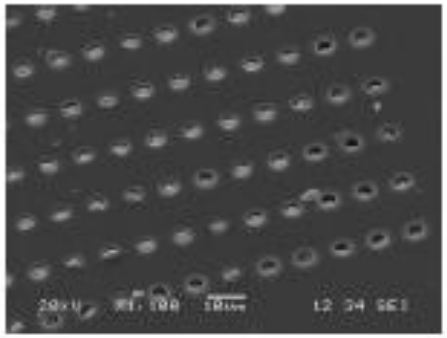
- How to test the interposer?
- Micro-bump probe access
  - Probe needles much larger than TSV/micro-bump size and pitch
- Probe card applies force (weight)
  - TSVs/microbumps have low fracture strength
- Post-bond access: No direct access to non-bottom dies
- New defects due to TSV manufacturing process



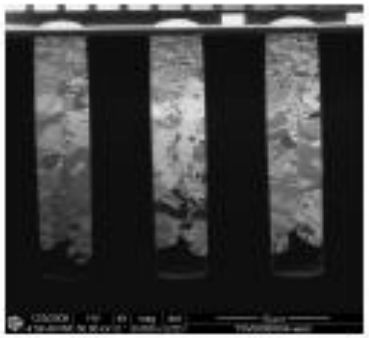
[IMEC]



TSV Defect

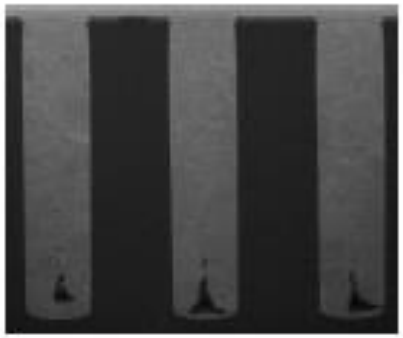


Improperly filled TSVs

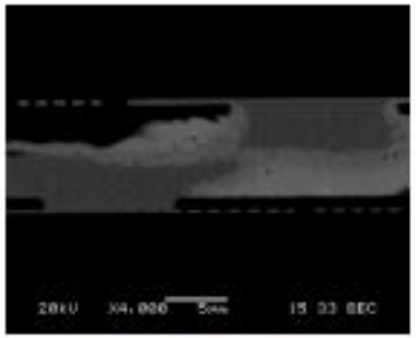


Insufficiently filled TSVs

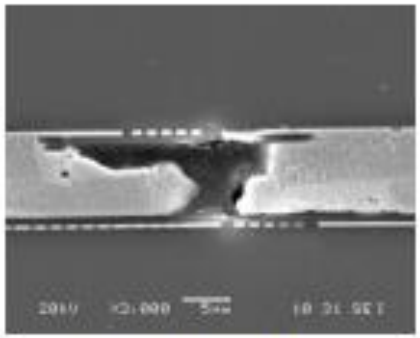
Micro-voids on TSV axis (quasi-conformal filling)



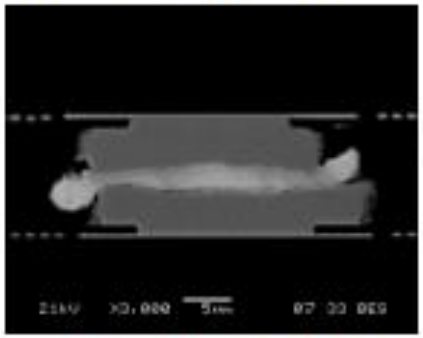
Micro-voids on TSV axis + large voids at bottom



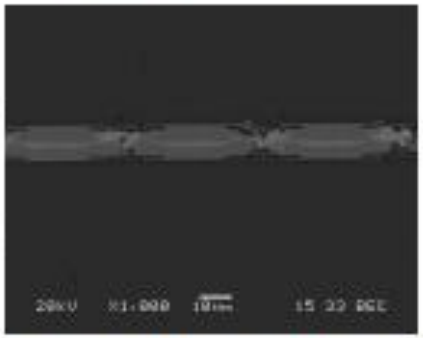
Misalignment



Misaligned bumps, almost-short with neighbors



Improperly soldered micro bumps

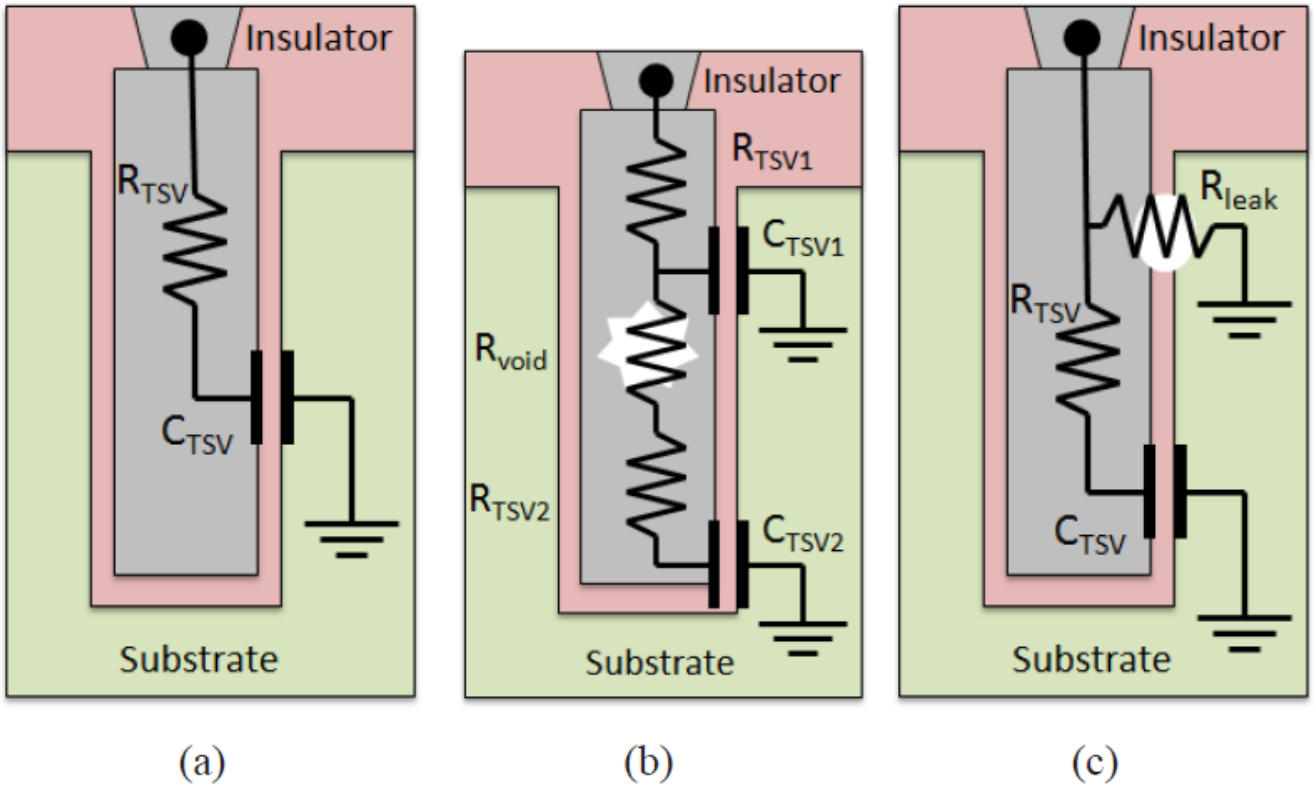


Shorts due to Sn squeezing

Examples of TSV Defects (IMEC, Belgium)

- How to test the TSVs? Pre-bond, post-bond
  - Underfill, pinhole defects, opens: pre-bond
  - Misalignment, mechanical/thermal stress: post-bond thermal effects

TSV Defects



(a) – Fault-free TSV

(b) – Resistive-open defect

(c) – Leakage defect

TSV Defects (Contd.)

Stress-induced defects

- Copper area
- Silicon area
- Overall area

Cu - area		Si - area	Overall area
Thermal mismatch (extrinsic stress) ⇩ ▪ TSV extrusion ▪ Debonding ▪ Bump crack & delamination	Rapid grain growth (intrinsic stress) ⇩ ▪ Void formation ▪ Void growth & coalescence ▪ Crack generation & propagation	Cu-induced residual stress ⇩ ▪ Change of carrier mobility	Bump process-induced stress ⇩ ▪ Plastic deformation & fracture in bump and soldering

G. Lee et al – 3DIC'12

Pre-Bond Testing of TSVs: Myth or Reality

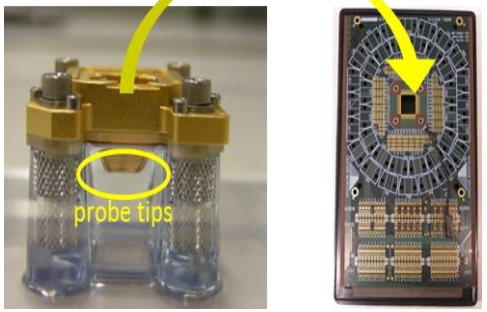
- Some semiconductor companies say no!
  - Too fragile, too difficult to test pre-bond
  - Process people will fix the yield problem!
  - "We deal with much larger number of vias through DFM rules, and TSVs are at least an order of magnitude larger…"
- But…
  - TSV defects affect surrounding silicon!
  - So more testing of die logic needed
  - Micro-bump defects not addressed as easily by process fixes
  - Probing solutions on the horizon

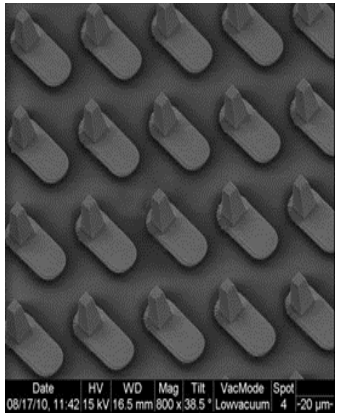
IMEC – Cascade Microtech

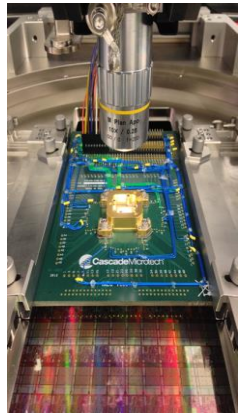
[Marinissen et al, ITC'14]

Cascade Microtech's Probe Technology

- Pyramid Probes® Rocking Beam Interp.
- MEMS-type thin-film probe card
- Lithographically-defined probe tips





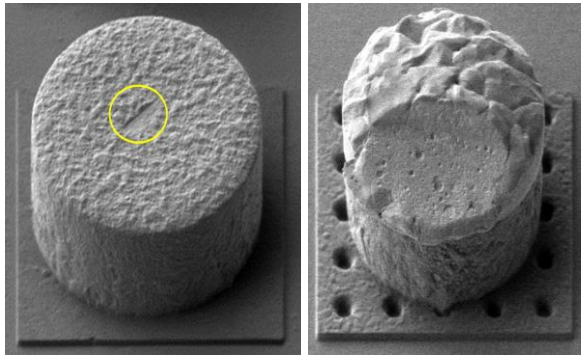


IMEC's 2.5D Test Chip 'Vesuvius-2.5D'

- Full four-bank JEDEC Wide-I/O interface (= 1,200 micro-bumps)
- Daisy-chains through micro-bumps

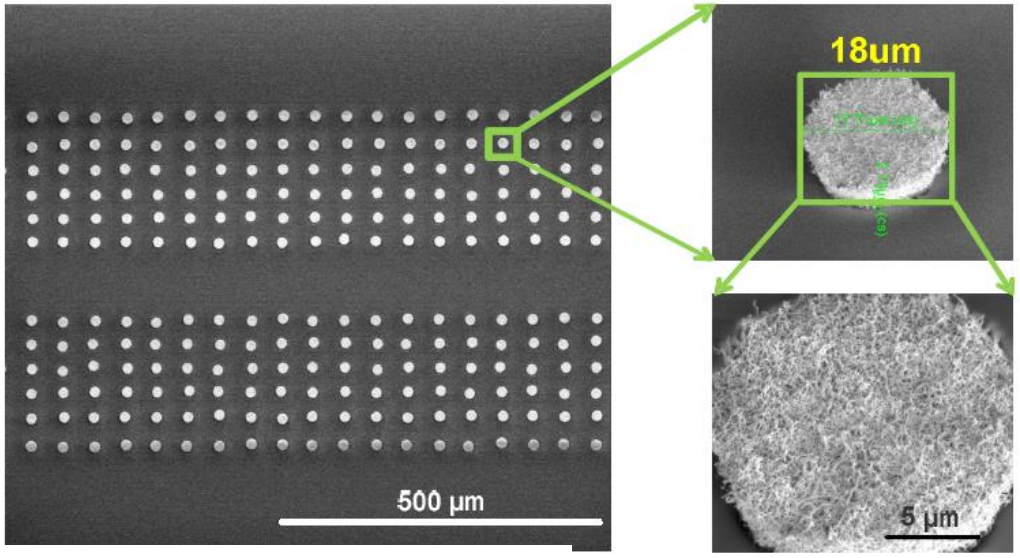
Demonstrated

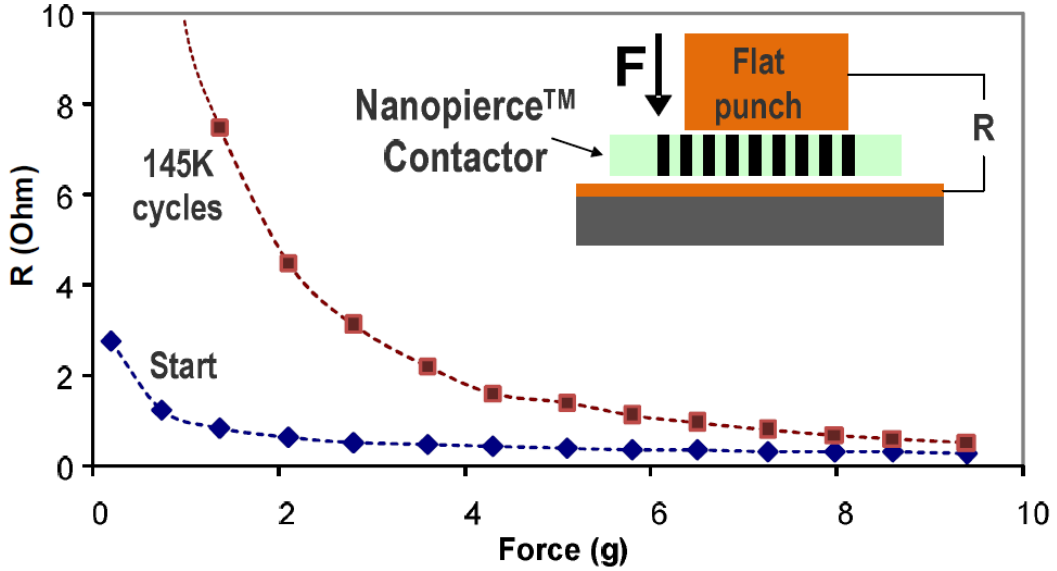
- Successful probing with single-channel Wide-I/O probe card on Cascade Microtech CM300 probe station
- Limited probe marks on micro-bumps: Cu and Cu/Ni/Sn (after reflow)
- No measureable impact of probing on stacking yield
- 3D-COSTAR: Economic feasibility in single-site testing



NanoPierce™ TSV Contact Solution (FormFactor)

- Socket contacts
- Down to 20 µm array pitch
- Flexible film with many nanofibers





Probing with "TSV Matrices" (Duke Univ.)

US008775108B2

(12) **United States Patent**
Chakrabarty et al.

(10) **Patent No.: US 8,775,108 B2**
(45) **Date of Patent: Jul. 8, 2014**

(54) **METHOD AND ARCHITECTURE FOR PRE-BOND PROBING OF TSVS IN 3D STACKED INTEGRATED CIRCUITS**

(75) Inventors: **Krishnendu Chakrabarty**, Chapel Hill, NC (US); **Brandon Noia**, Durham, NC (US)

(73) Assignee: **Duke University**, Durham, NC (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 392 days.

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Noia and Chakrabarty, *IEEE Trans.CAD*, 2013

TSV Probing for Die Logic Testing (Duke Univ.)

(12) **United States Patent**
Chakrabarty et al.

(10) **Patent No.: US 8,782,479 B2**
(45) **Date of Patent: Jul. 15, 2014**

(54) **SCAN TEST OF DIE LOGIC IN 3D ICS USING TSV PROBING**

(71) Applicant: **Duke University**, Durham, NC (US)

(72) Inventors: **Krishnendu Chakrabarty**, Chapel Hill, NC (US); **Brandon Noia**, Durham, NC (US)

(73) Assignee: **Duke University**, Durham, NC (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 128 days.

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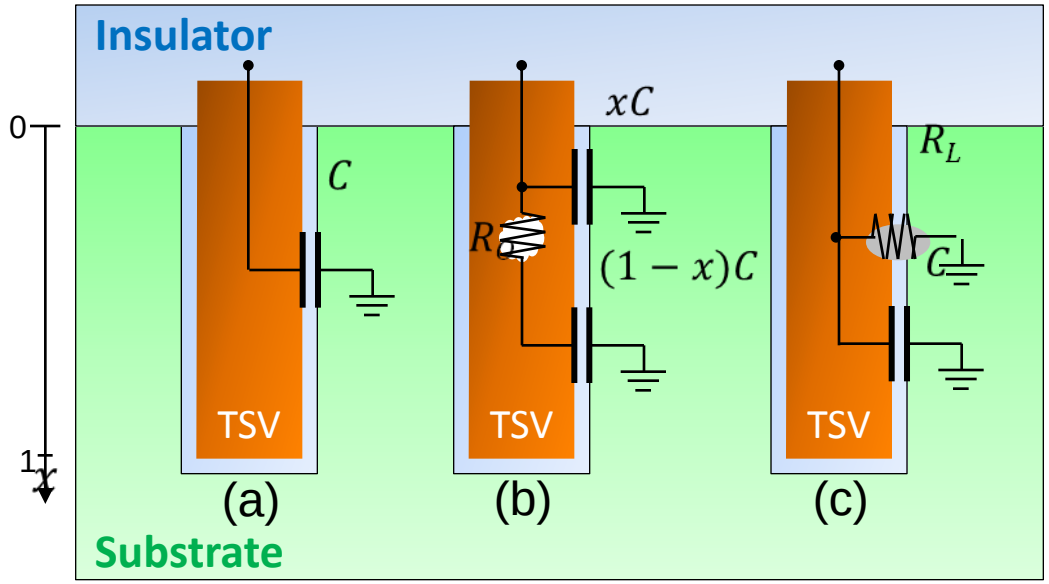
Chakrabarty and Noia, "Pre-Bond Probing of TSVs in 3D Stacked ICs," Test Conference (ITC), 2011 IEEE International, Sep. 20-22, 2011.

* cited by examiner

Noia et al., *IEEE Trans. VLSI Systems*, 2015

Non-Invasive Pre-Bond TSV Test

(*Deutsch and Chakrabarty, TCAD 2014, ITC 2015*)



$C = 60$ fF
$R_O = 0 \ldots 3$ kΩ
$R_L = 0 \ldots 10$ kΩ

a) Fault-free case: lumped capacitor $C = 60$ fF
($R_{TSV} < 1$ Ω → neglect R_{TSV})

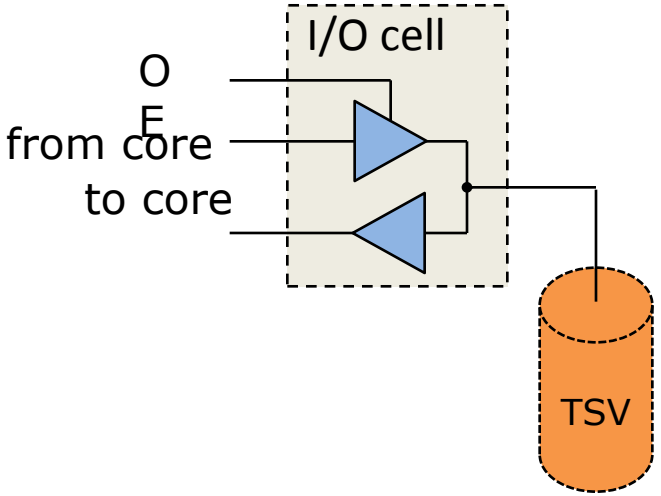
b) Resistive open fault: $R_O = 0 \ldots 3$ kΩ at the location x

c) Leakage fault: $R_L = 0 \ldots 10$ kΩ

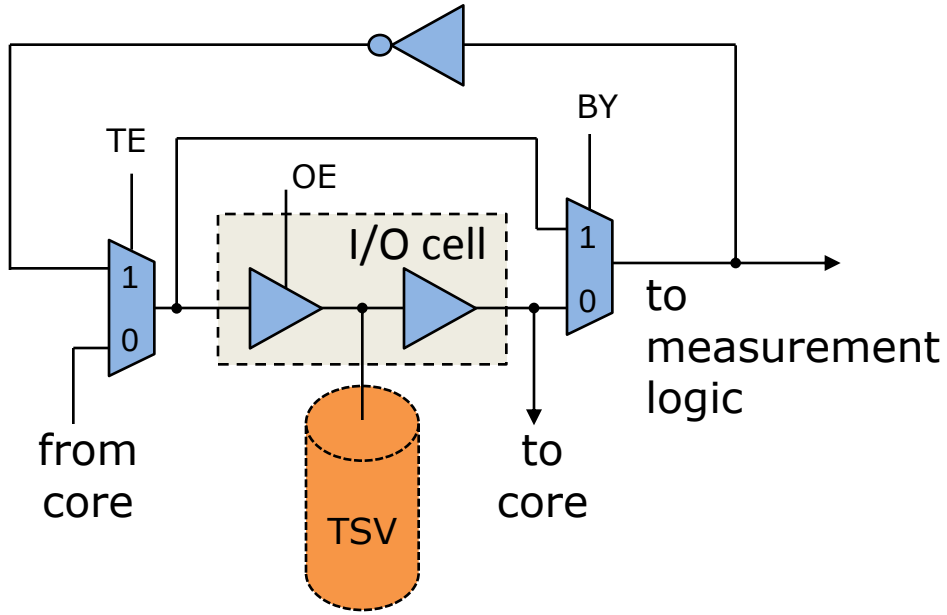
Main idea: parametric test for R_O and R_L

Ring Oscillator Configuration

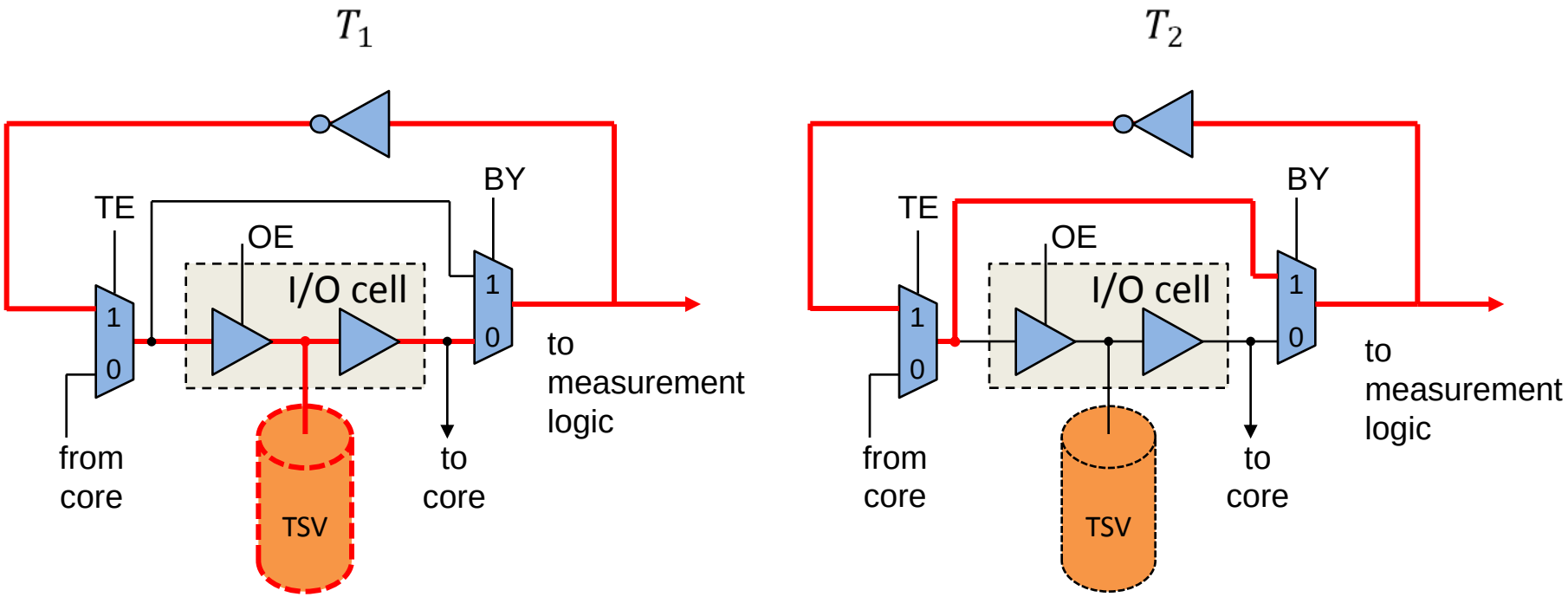
Functional circuitry:



Design-for-Test extension:



Ring Oscillator Configuration



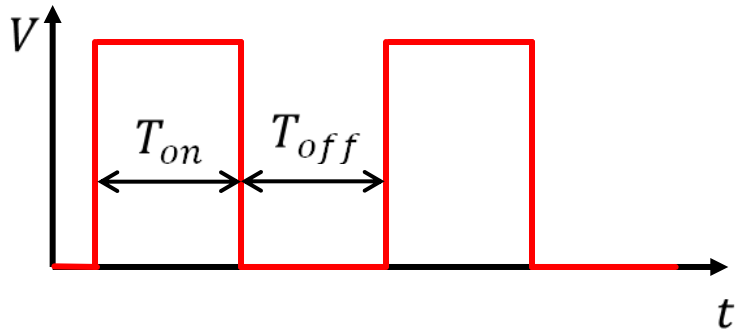
- Measure difference $\Delta T = T_1 - T_2$ to reduce inaccuracy due to random process variations
- ΔT sensitive to defects in TSVs
  - ΔT⬇ if resistive open
  - ΔT⬆ if leakage

Using Duty Cycle for Pre-Bond TSV Test

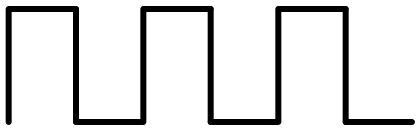
Definitions:

Oscillation period: $T_{osc} = T_{on} + T_{off}$

Duty cycle: $D = \frac{T_{on}}{T_{on}+T_{off}}$

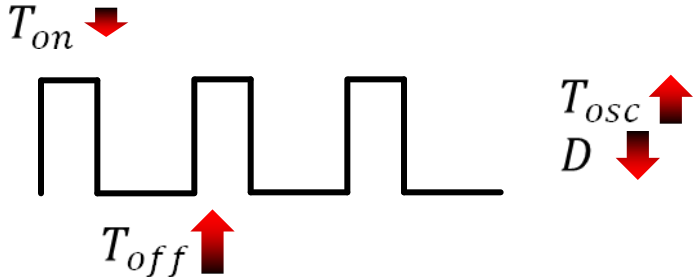


Fault-free
$(G_L = 0, R_O = 0)$

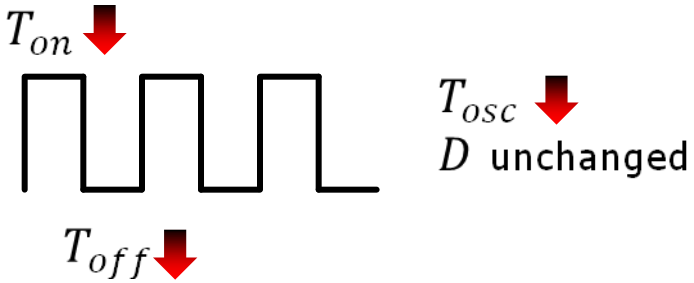


$D \approx 0.5$

Leakage fault
$(G_L > 0)$



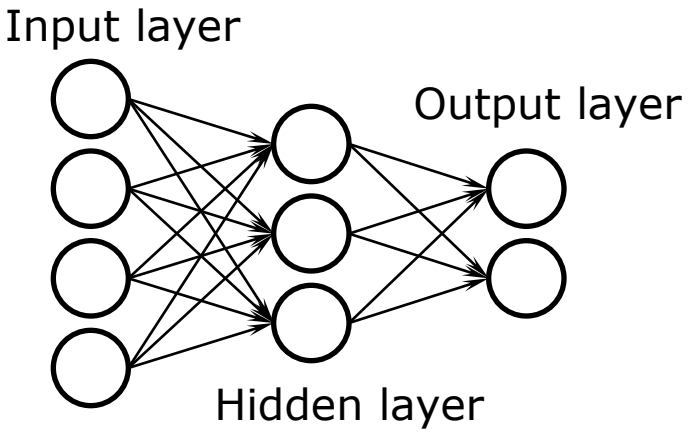
Resistive-open
fault $(R_O > 0)$



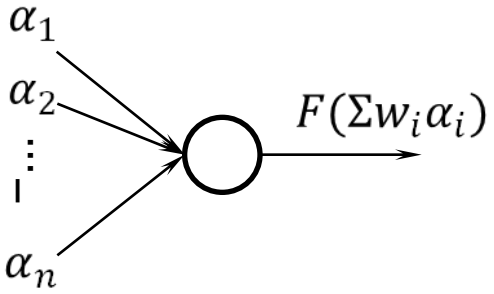
Regression Model Based on Artificial Neural Networks

- **Objective**: determine **fault type and size** based on measurements
- Use artificial neural networks (ANNs):
  + Efficient for complex systems with large number of inputs
  – Require sufficient number of samples for training

Generic ANN architecture:



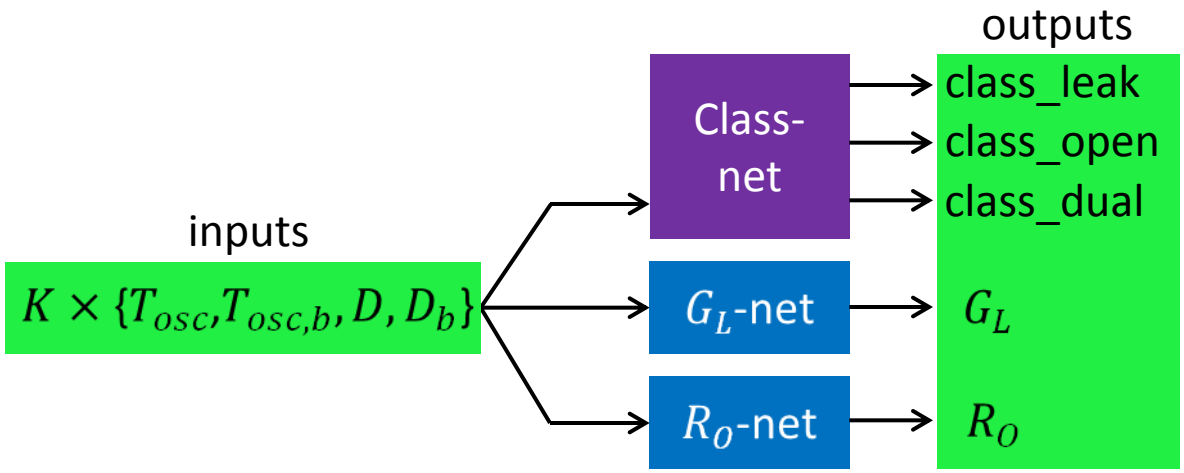
Neurons:



Common transfer functions:

- Pure linear $F(\xi) = \xi$
- Sigmoid $F(\xi) = \frac{1}{1+\exp(-\xi)}$

Regression Model Based on ANN



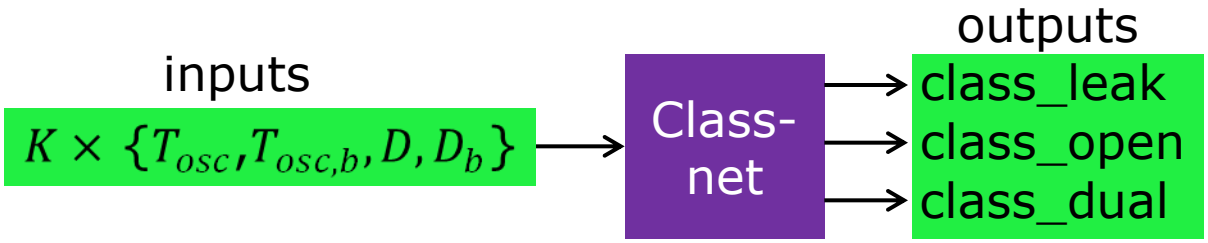
- Class-net: classification network to determine fault type
- G_L-net: function-fitting network to determine G_L
- R_O-net: function-fitting network to determine R_O

- Inputs: $\{T_{osc}, T_{osc,b}, D, D_b\}$ measured at ***K*** voltage levels

Regression Model: Simulation Results

- Two sets of training and test data (10,000 MC samples each)
- $K = 8$ ($V_{dd} = 0.85 \ldots 1.2V$)
- G_L from 0 (fault-free) to 450 µS (strong leakage)
- R_O from 0 (fault-free) to 5000 Ω (strong resistive open)

Evaluation of Class-net



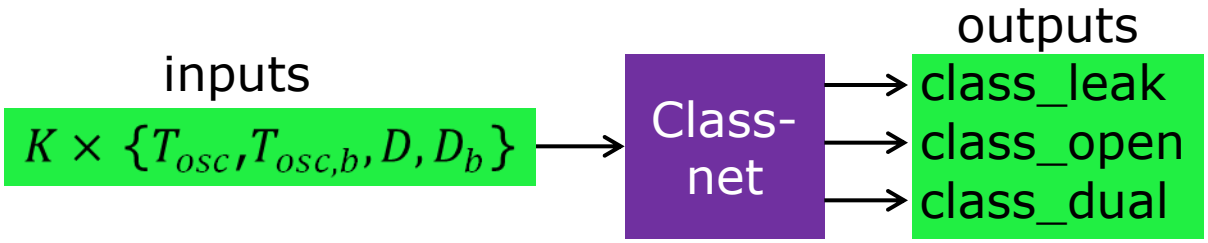
Evaluation steps:

1. Train Class-net using training sample set

2. Predict fault class using Class-net for evaluation sample set

3. Compare output class with actual (target) class for each sample

Evaluation of Class-net



Confusion matrix:

Target Class

Output Class	class_leak	class_open	class_dual
class_leak	9524 33.3%	58 0.2%	0 0.0%
class_open	37 0.1%	9818 34.4%	135 0.5%
class_dual	0 0.0%	124 0.4%	8865 31.0%

Correct prediction

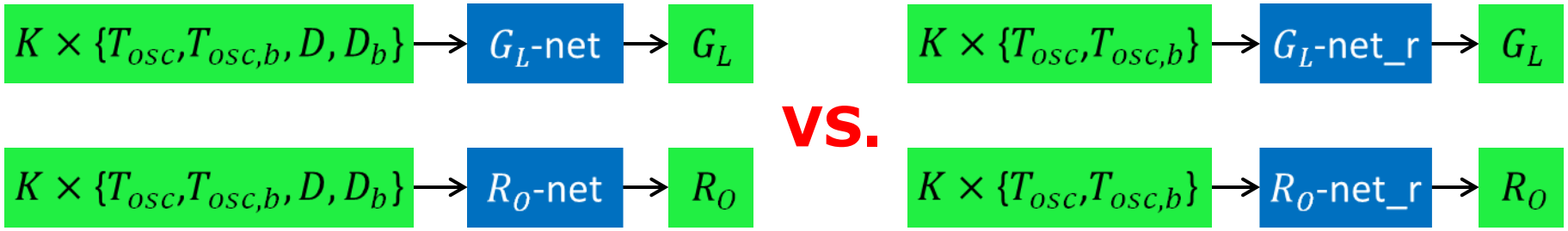
Misprediction

→Number of mispredictions is relatively small

Evaluation of G_L-net and R_O-net

T_{osc} alone good enough as input parameter?

- Comparison with models using only oscillation period
- All models trained using same training data set



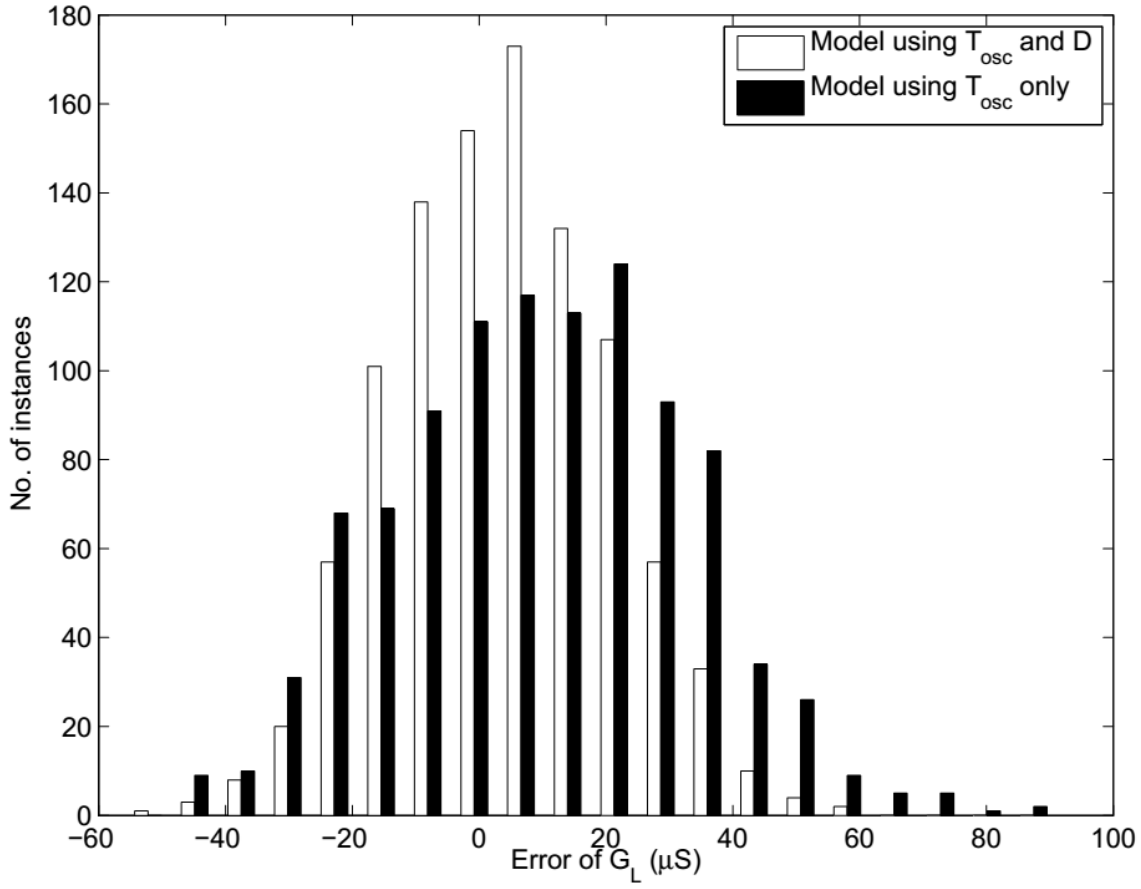
- Performance evaluation metric: mean squared error (MSE)

$$\mathrm{MSE} = \frac{1}{N}\sum_{i=1}^{N}(y_{p,i} - y_{t,i})^2$$

  - $y_{p,i}$ target value
  - $y_{t,i}$ predicted value

Evaluation of G_L-net

Error histograms of G_L-net and G_L-net_r at G_L = 100 µS.

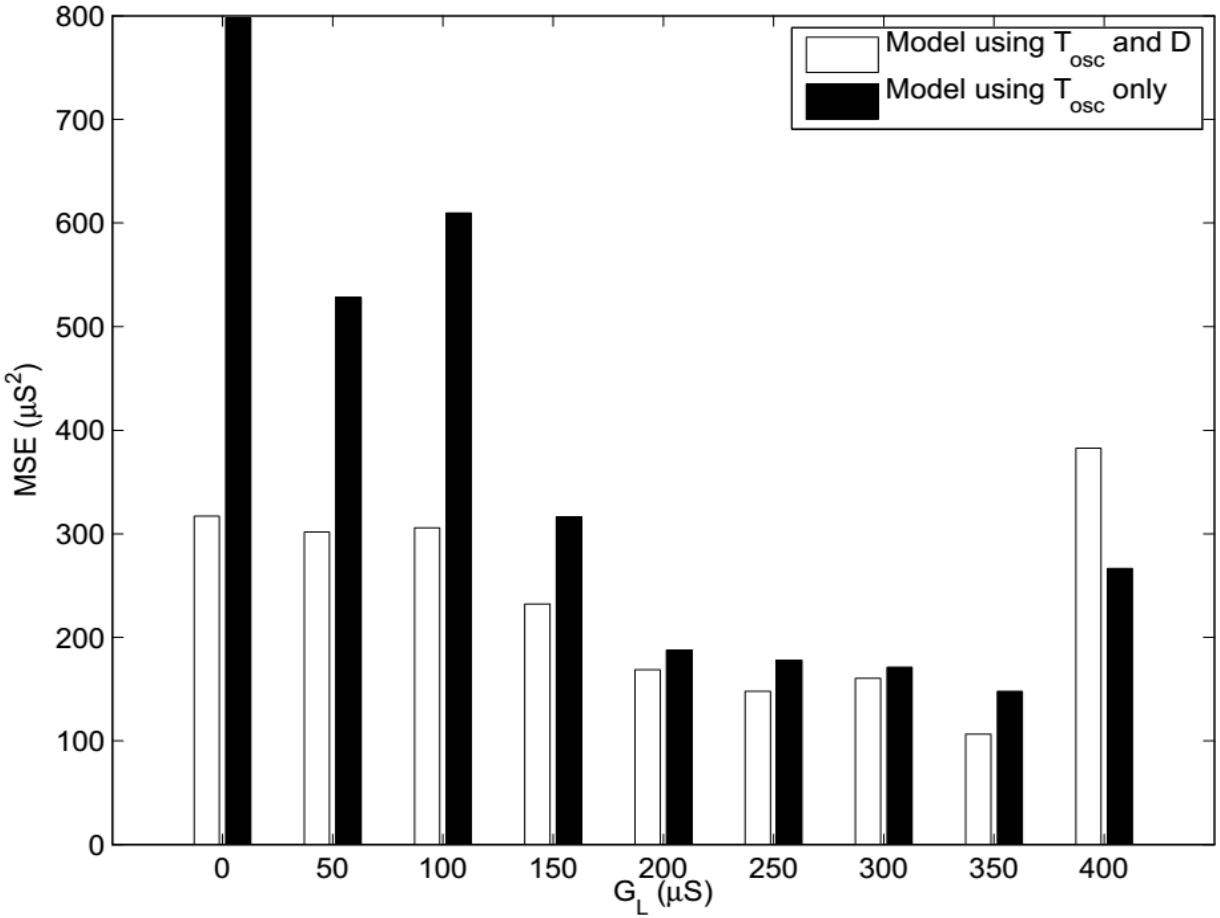


Error = $y_{p,i} - y_{t,i}$

→ G_L-net more accurate (less spread around zero error)

Evaluation of G_L-net

- MSE of G_L-net and G_L-net_r for different values of G_L.



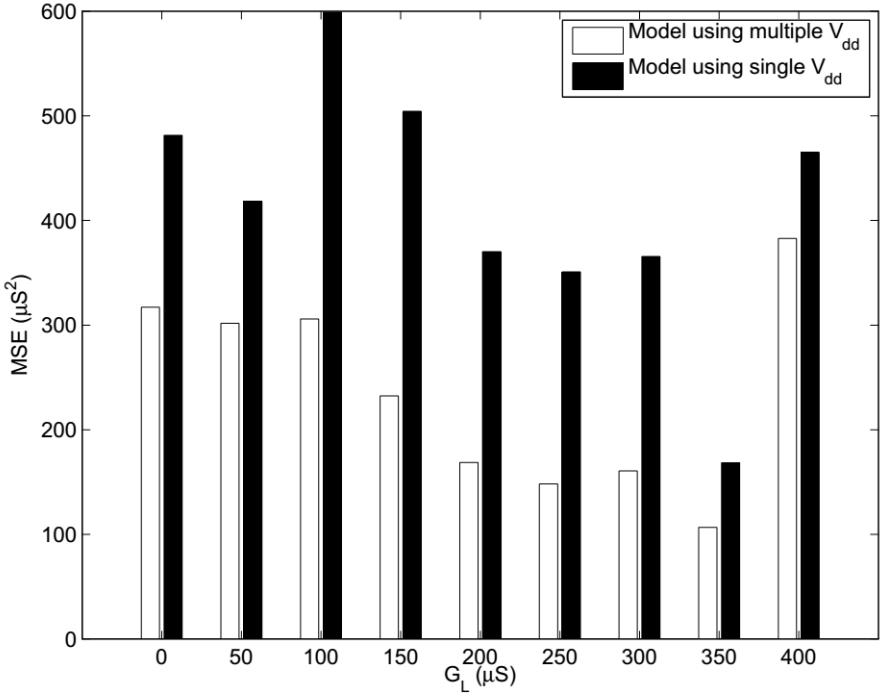
$$\mathrm{MSE} = \frac{1}{N}\sum_{i=1}^{N}(y_{p,i} - y_{t,i})^2$$

→ using *D* as additional input increases diagnosis accuracy for weak leakage (<100 μS)

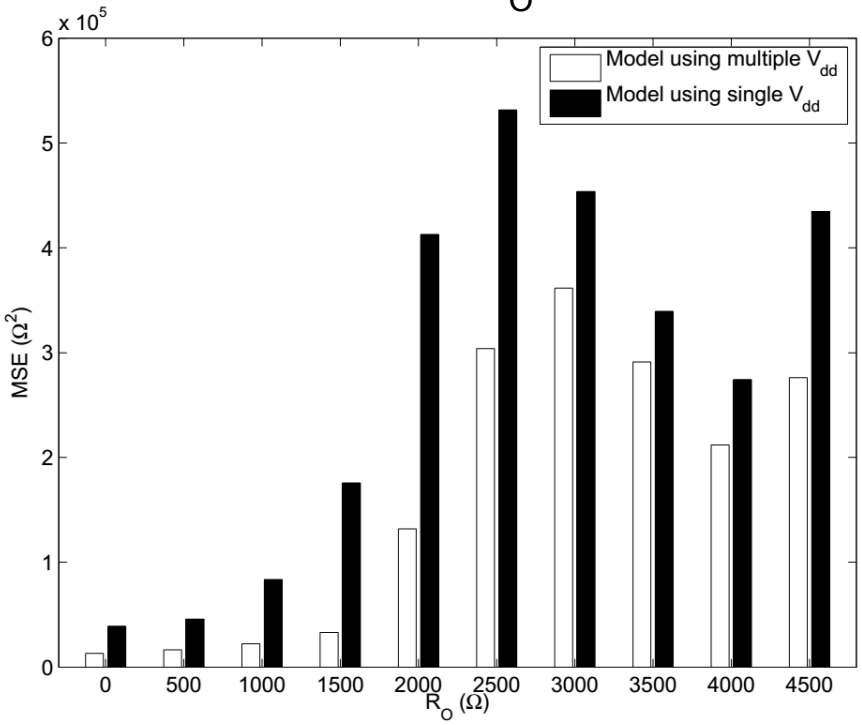
Multiple vs. Single V_{dd}

Do we need to test at multiple voltage levels?

MSE of G_L-net



MSE of R_O-net

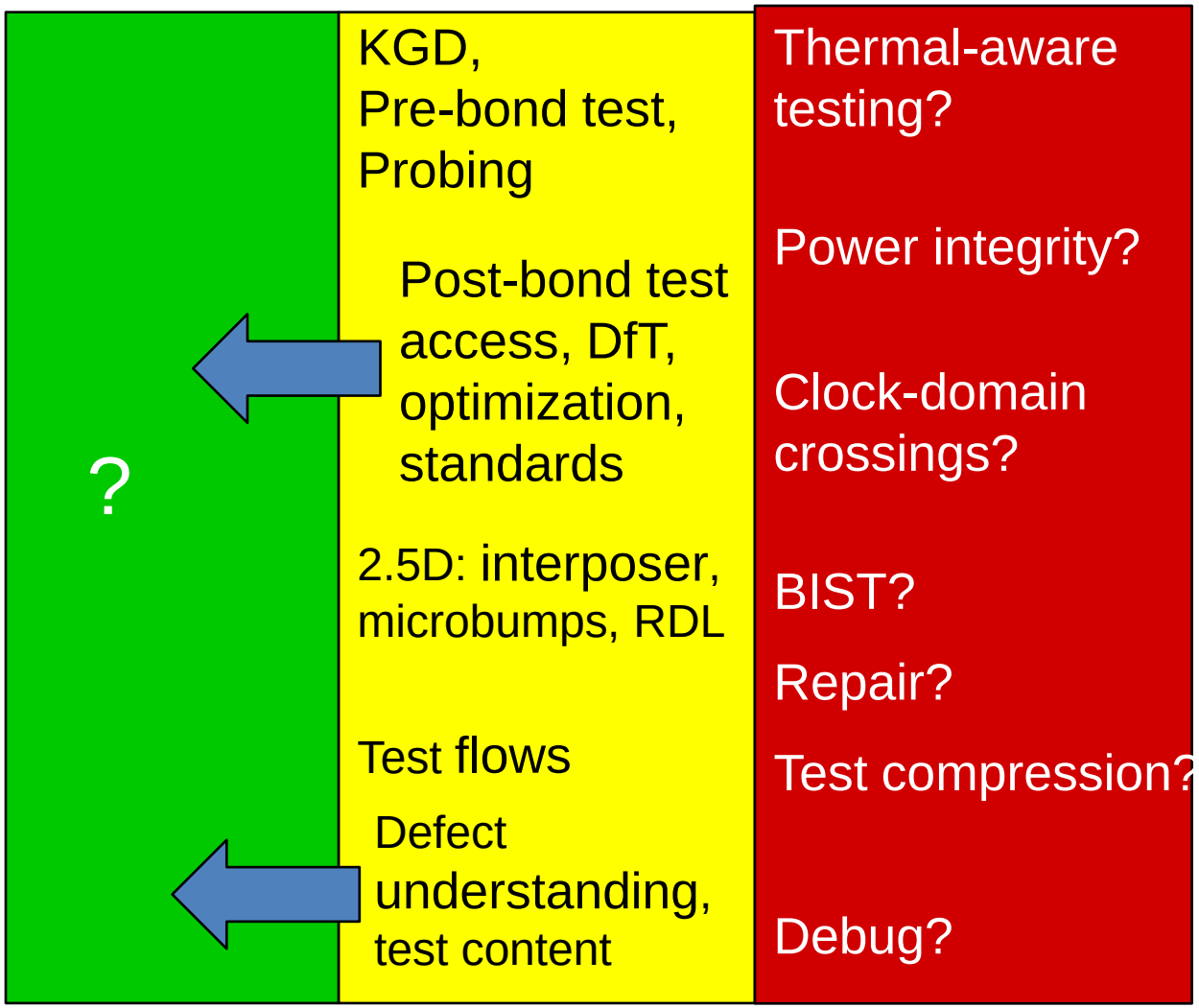


→ improved diagnosis accuracy using multiple voltage levels

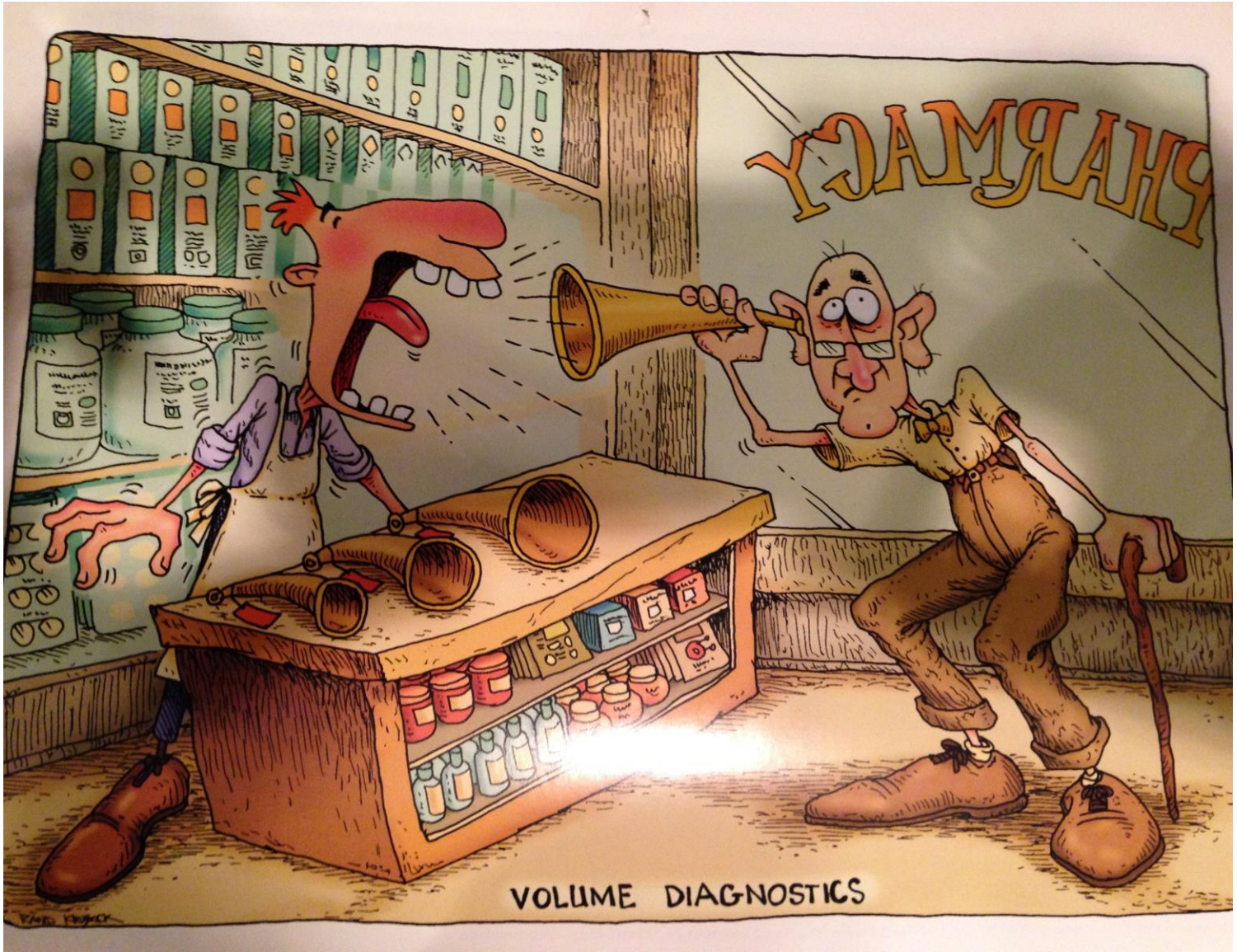
Conclusions

- 3D fabrication and assembly steps (TSVs, alignment, bonding, thinning, etc.) lead to unique defects
- Known test methods can be utilized (extended) for some problems
  - Post-bond test access, IEEE P1838
- Out-of-the-box thinking needed for other test challenges
  - Pre-bond testing (KGD, TSV testing, die logic testing)
  - Cost modeling (when and what to test)

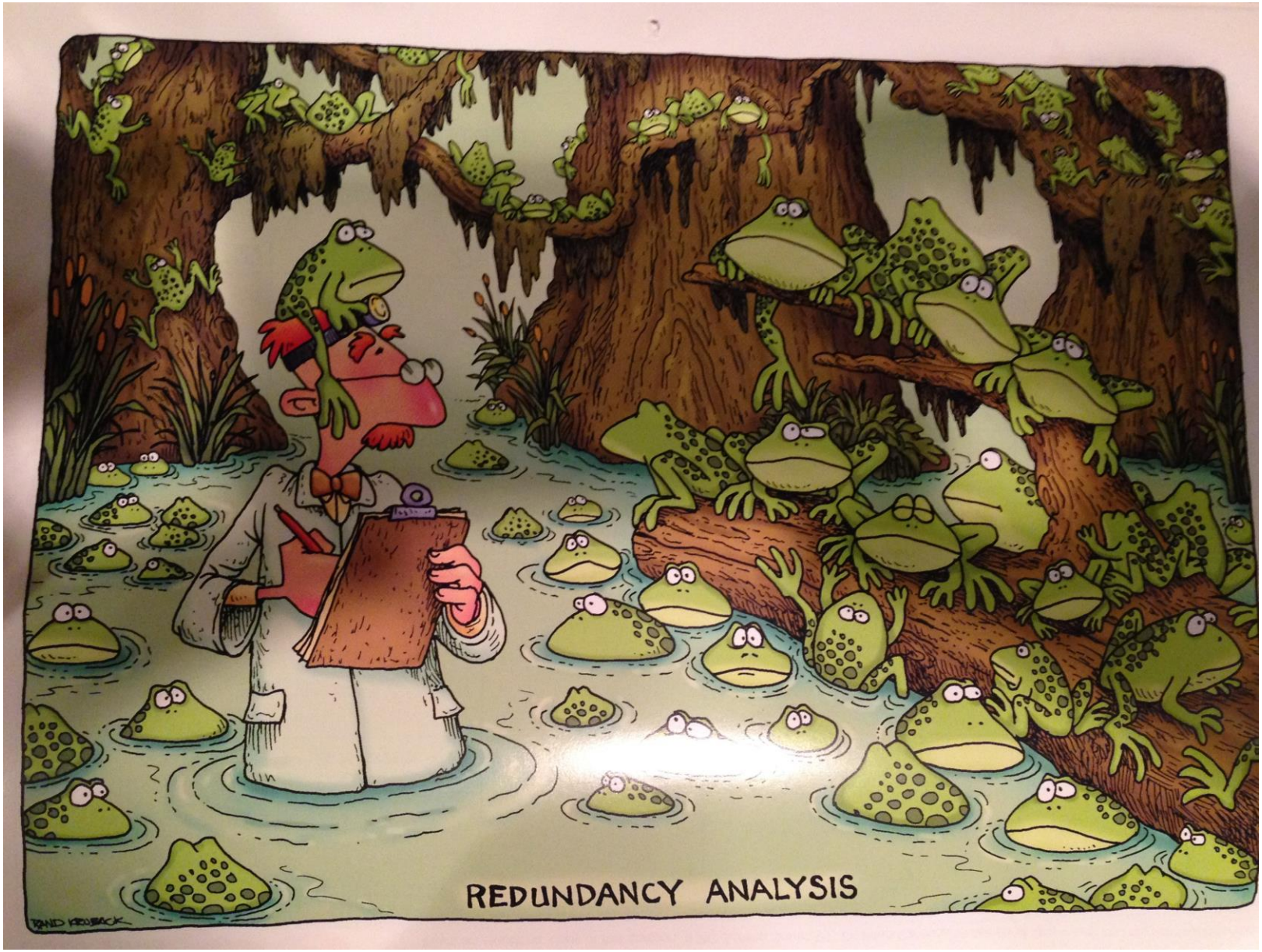
Traffic Lights



Target TSVs in Production Test and Volume Diagnostics?



TSV Redundancy?



Yield Learning for a 3D Stack?