Reliability Challenges in Through-Silicon Via (TSV)-Based Packaging

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October 29, 2015

Agenda

- Problem Statement
- Interconnect Reliability – Background
- TSV BIST Detection Approaches
  - SJ BIST
  - Built-in Current Monitoring
- Summary

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Existing Approaches to 2.5D/3D IC Test

- "Known Good Die" → "Pretty Good Die"
- Finding Defects Prior to Shipment
  - X-ray, Optical Inspection
  - Boundary Scan (IEEE 1149.x)
  - IEEE P1838, others
- Limited Focus
  - Opens & shorts
  - Primarily digital
  - Static / low speed operation
  - Intermittencies?
  - Continuous / Life-time assessments ?
  - Thermal issues?... Assembly complexities?...
- …Reliability = Performance *Over Time*

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Intermittencies

- Reported electronic system problems in the field cannot be duplicated at the service point or in the lab
- “Three/Four-letter” words (CND, NTF, RTOK)
  - Could Not Duplicate (CND)
  - No Trouble Found (NTF)
  - Retest OK (RTOK)
- 50 to 80% of these CND/NTF/RTOK problem categories are reported by service personnel.
- Major culprits
  - Interconnect intermittencies
  - NBTI effects in deep submicron ICs

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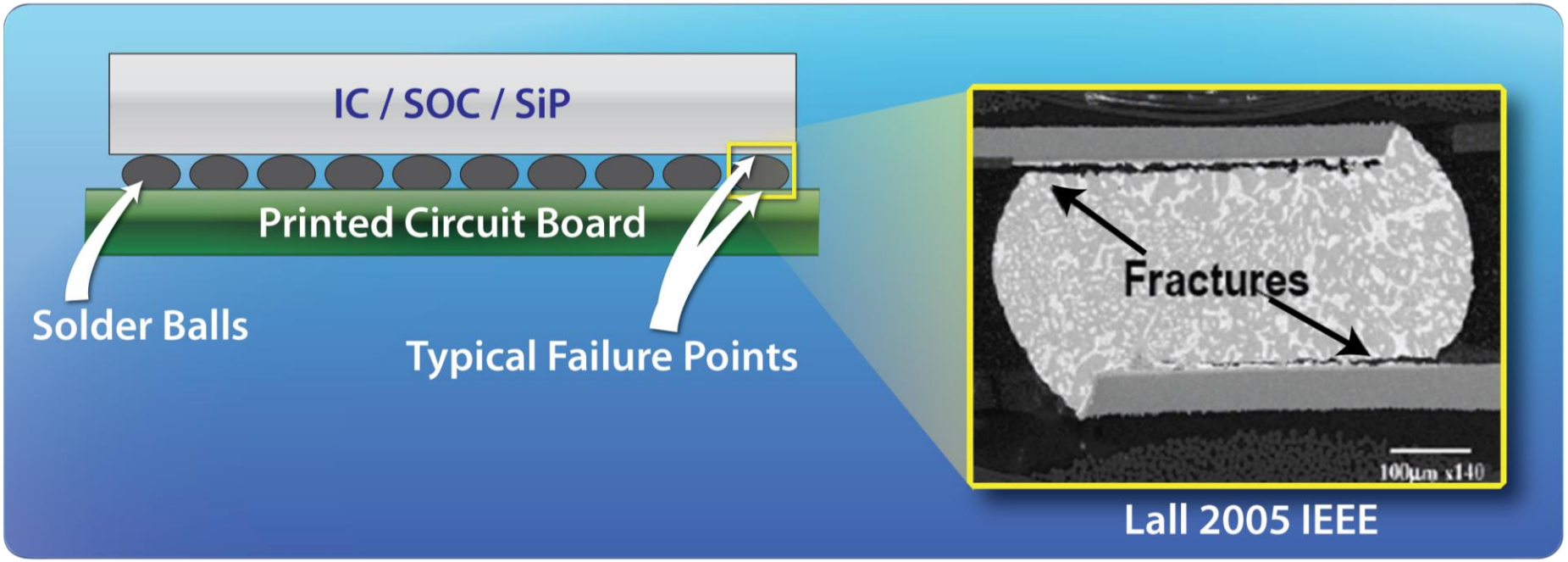
BGA Example: Cracks and Fractures



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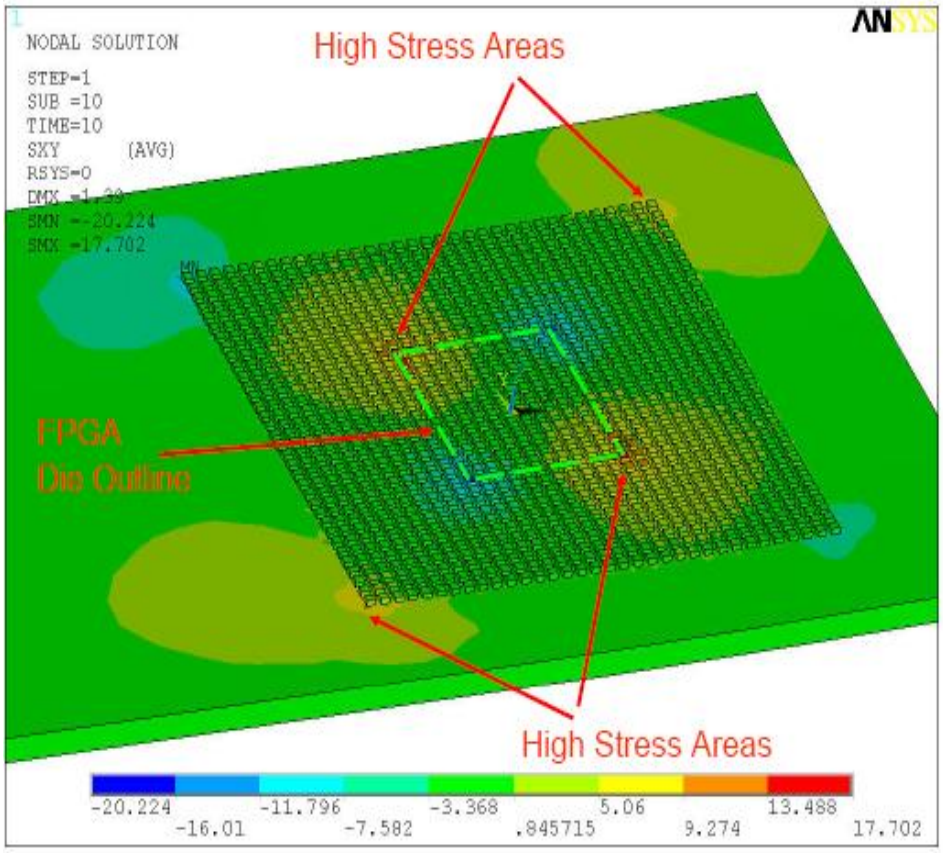
Defects: Location of Cracks/Fractures

- Corner pins likely to fail first
  - High stress areas, and corners of the package and die



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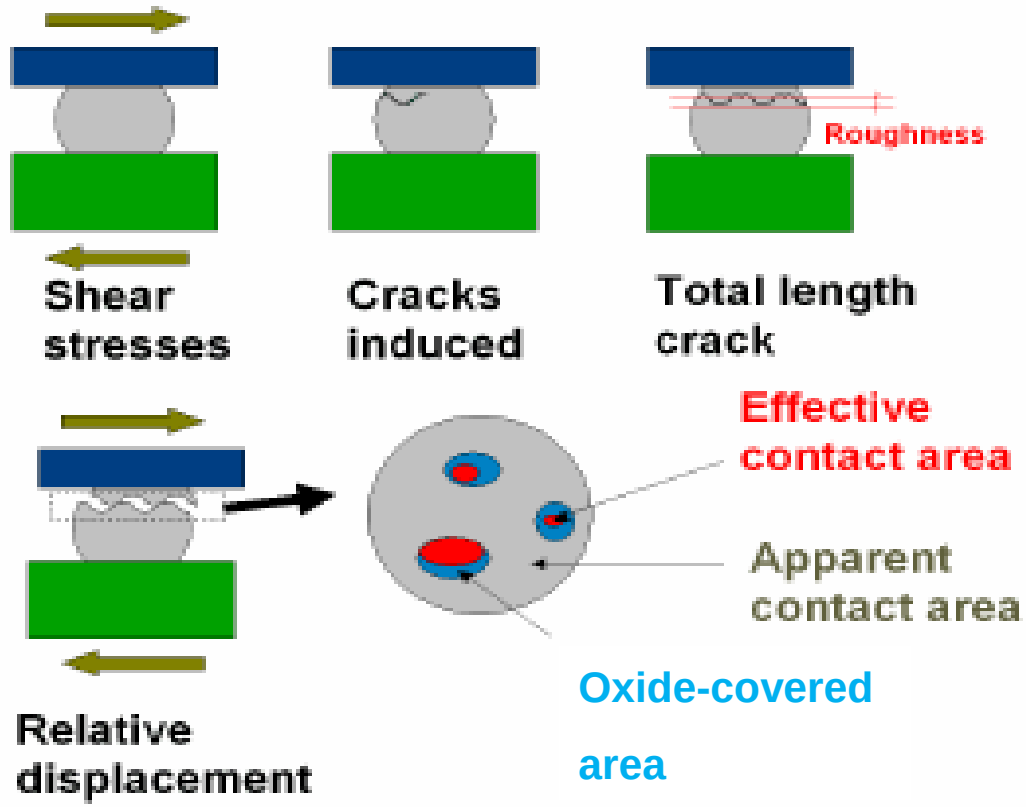
Mechanisms of Failure

- Fatigue fractures (cracks) are caused by thermo-mechanical stress/strain
- During periods of high stress, fractured bumps tend to momentarily open and cause intermittent faults of high resistance for periods of ns to µs
- Over time, contamination and oxidation films occur on the fractured faces: the effective contact area becomes smaller and smaller
- Transient opens can be detected by event detectors



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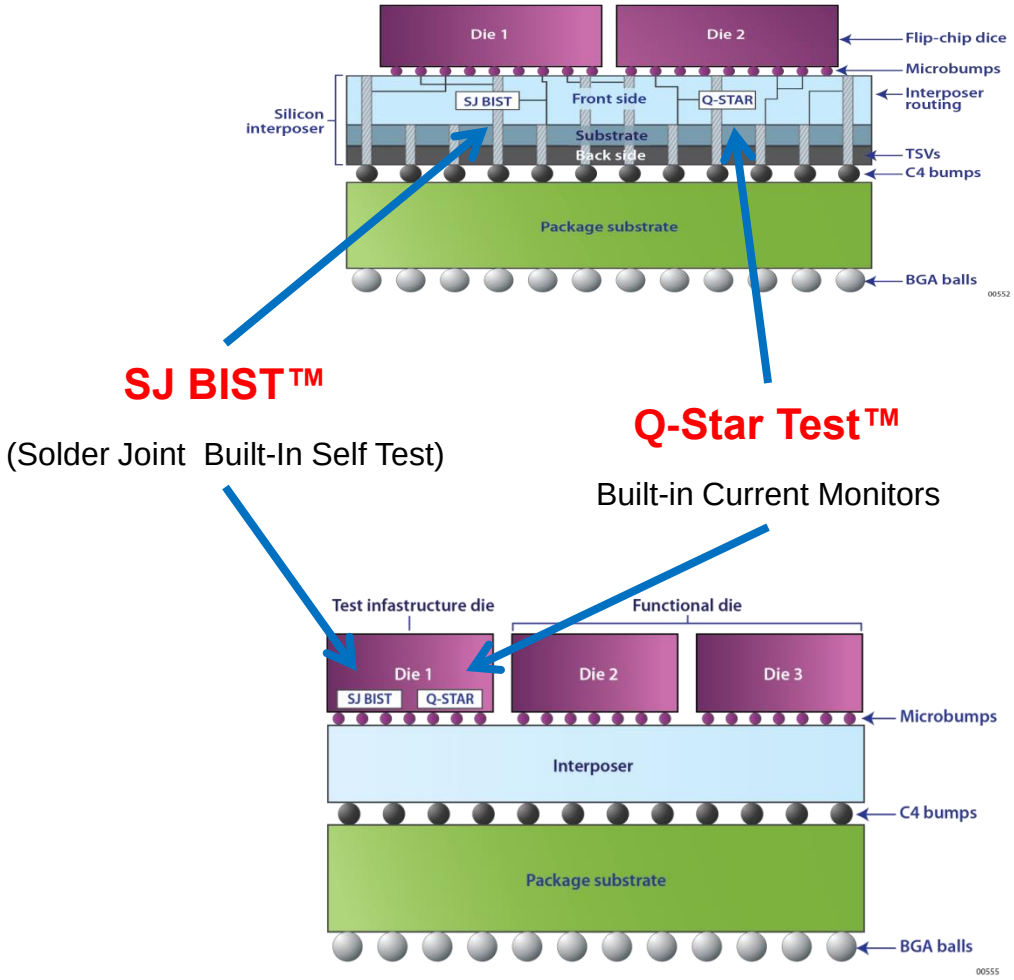
Ridgetop 2.5D/3D IC Reliability System

- Proven BIST methodologies
- Real-time monitoring of interconnection integrity
  - Monitors degradation
  - Warns of impending failure (prognostic "canary cell")
  - Detects and identifies intermittencies
- Covers both analog and digital signals
- Two alternate approaches (discussed in detail later)



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What is SJ-BIST?

- SJ BIST = Solder Joint Built-in Self-Test
  - Original solution, enabling:
    - interconnect verification
    - validation of interconnect reliability
    - (life-time) monitoring of interconnect reliability
    - detection of intermittences
    - interconnect process qualification
  - Originally developed for FPGA-BGA applications
  - Can be applied to validate the integrity and reliability of ***any type*** of interconnect
  - Soft core, can be instantiated in HW using Verilog or VHDL or in assembler to run on a MCU or CPU

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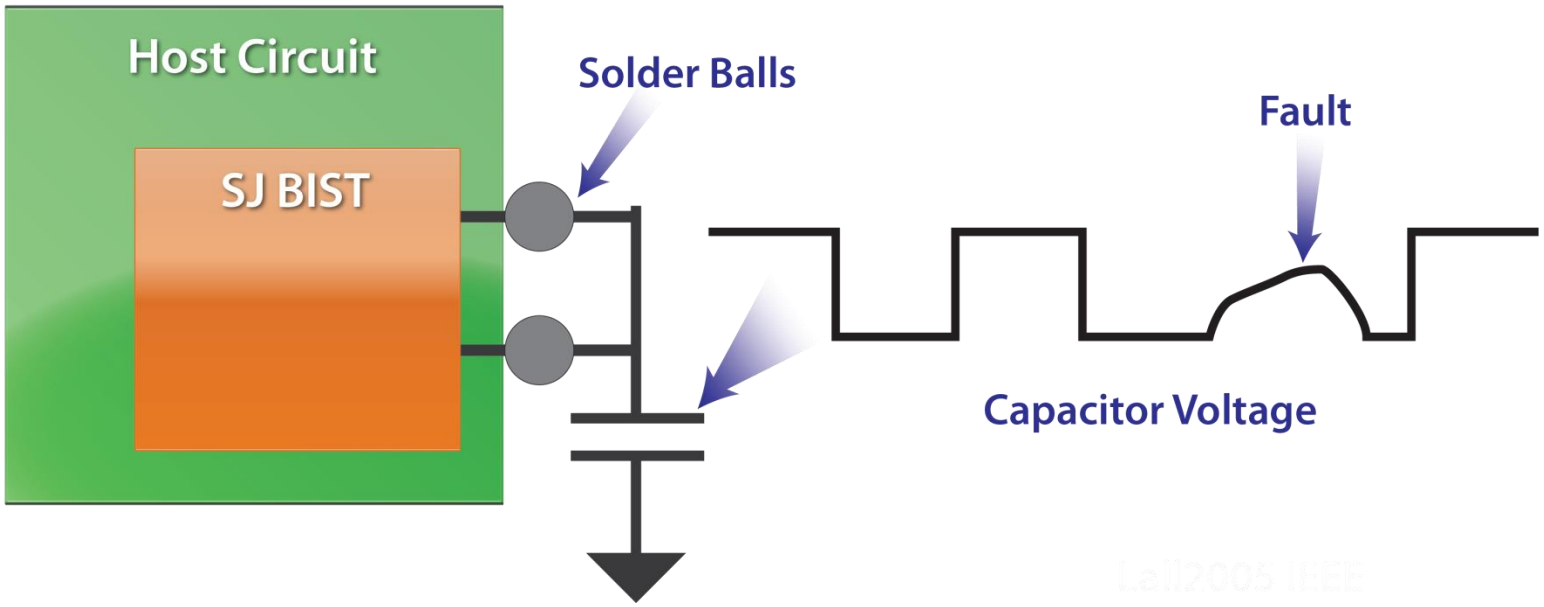
SJ BIST™ Operation

- Similar to a simple memory test: W0 – R0; W1 – R1
- Runs concurrently with host circuit
- Verilog/VHDL core (patent pending)
  - Each core tests two I/O pins
  - Pins are externally wired together
  - Small capacitor connected to the two pins



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SJ BIST Concept

- Interconnect == Memory
  - Connection between two dedicated pins
- Storage element == Capacitance of interconnect
  - Intrinsic (parasitic) capacitance of wire
  - I/O input capacitance
  - Small add-on capacitance
- Test == Transfer Charge == Memory Test
  - Write 0's and 1's
  - Verify if 0's and 1's are correctly stored

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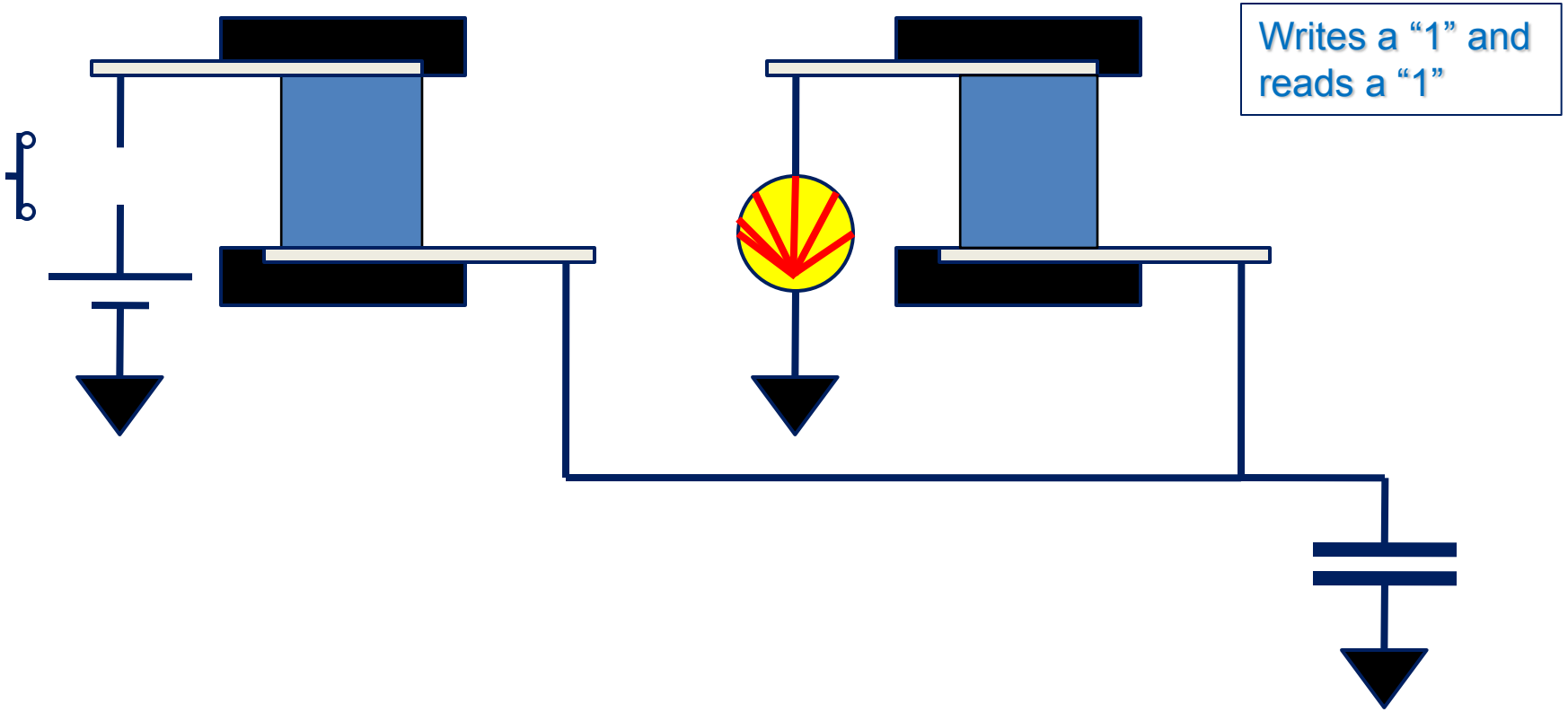
SJ BIST Operation

Healthy Connection



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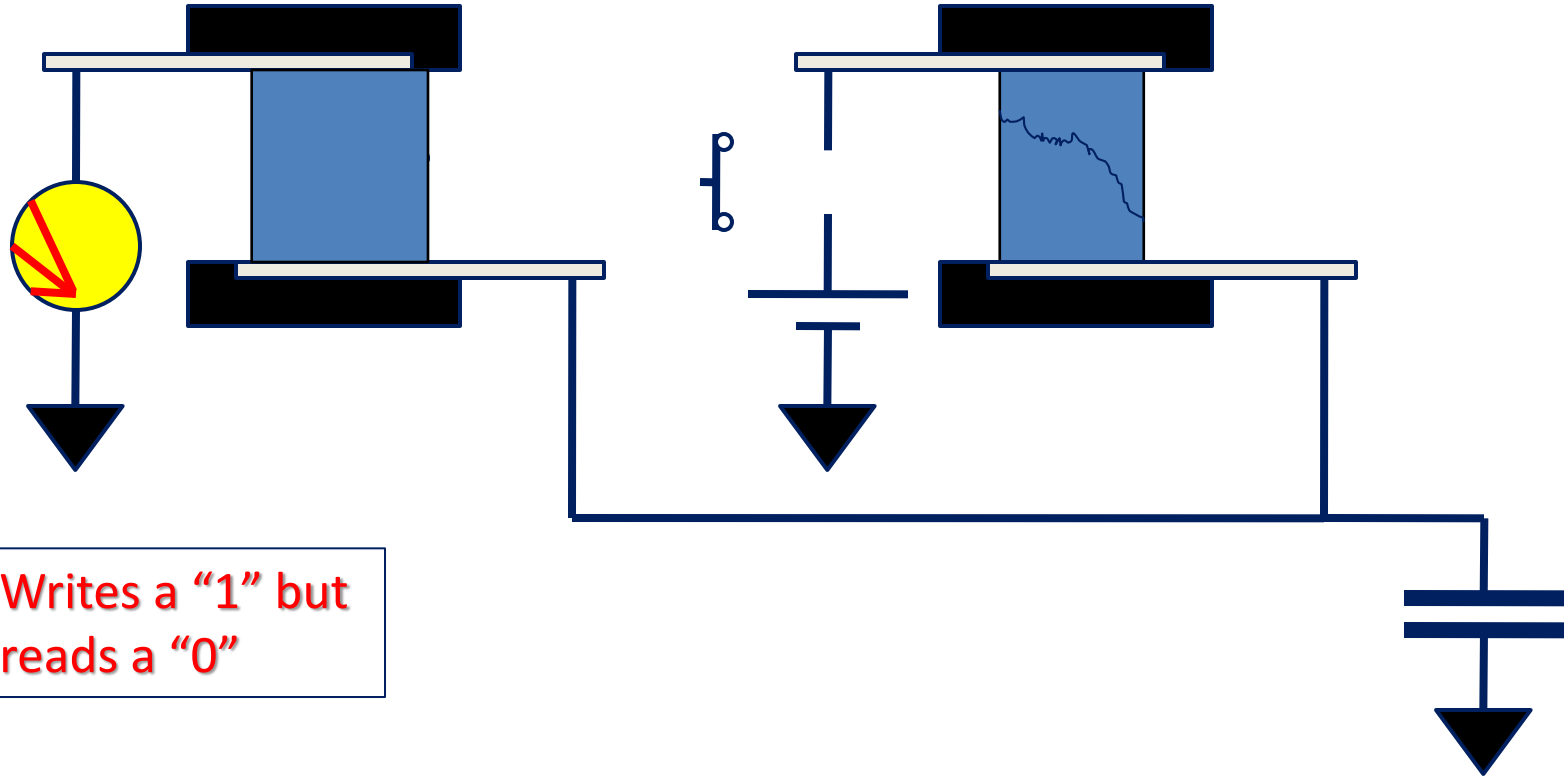
SJ BIST Operation

Faulty Connection



Writes a “1” but reads a “0”

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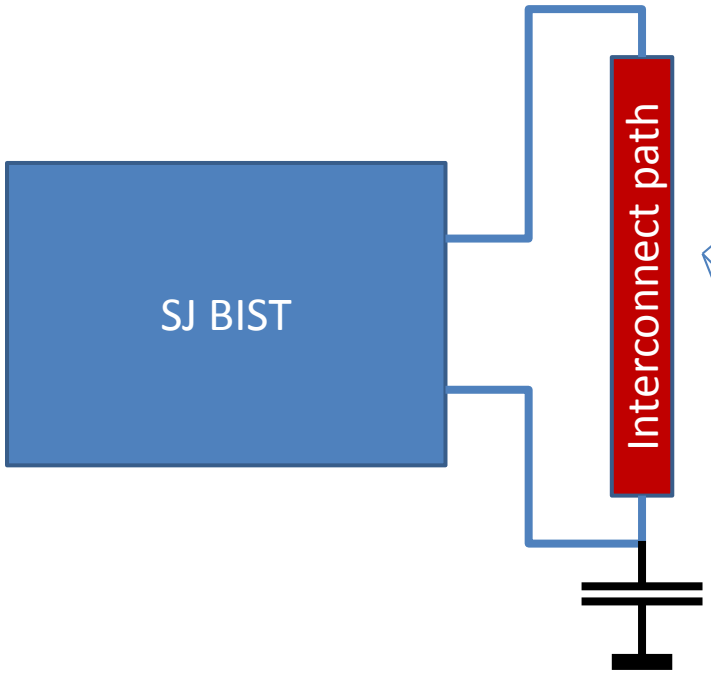
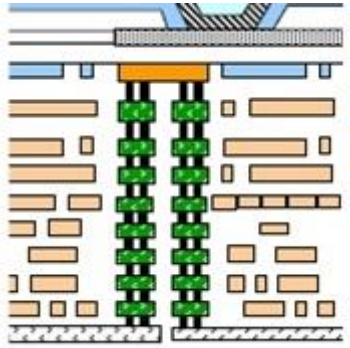
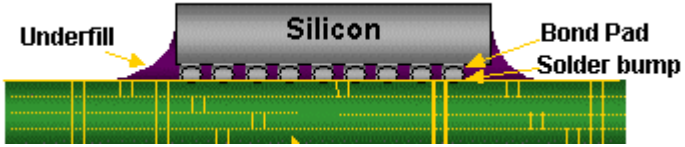
SJ BIST Application

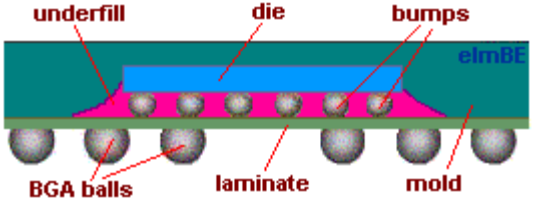




On-chip interconnects



Die to substrate (incl. bumps)



Die to board (incl. bumps & balls)

Requirement:
Interconnect path dedicated for SJ BIST

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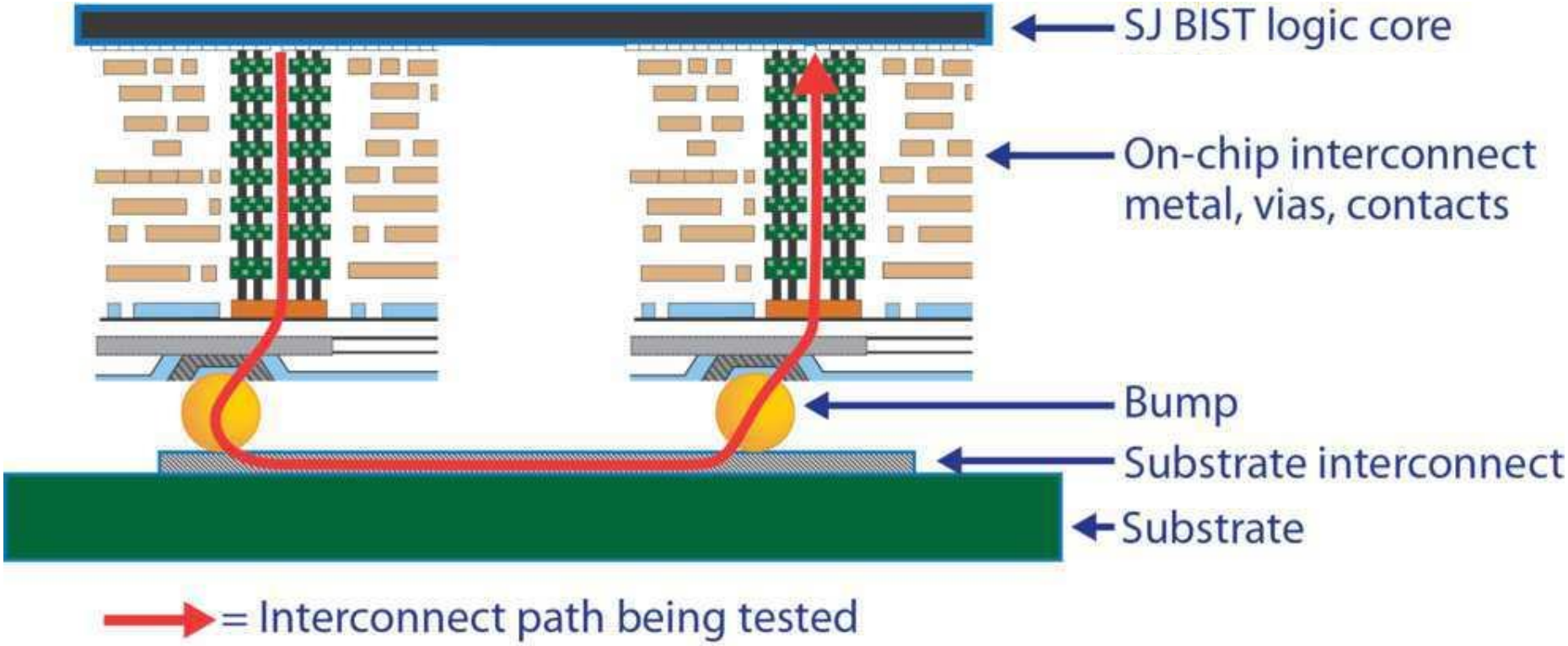
SJ BIST Application

Testing Die to Substrate



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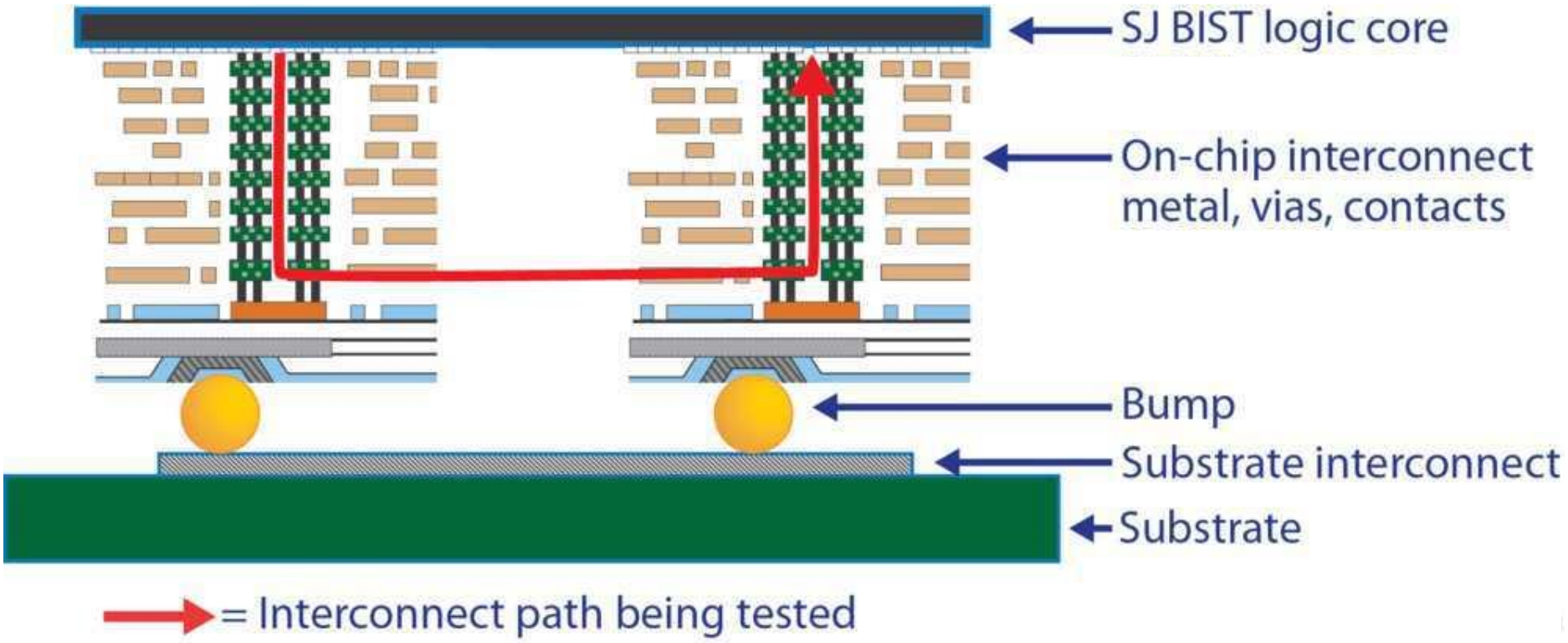
SJ BIST Application

Testing On-chip Interconnect



Need for dedicated on-chip path between SJ BIST observation pins

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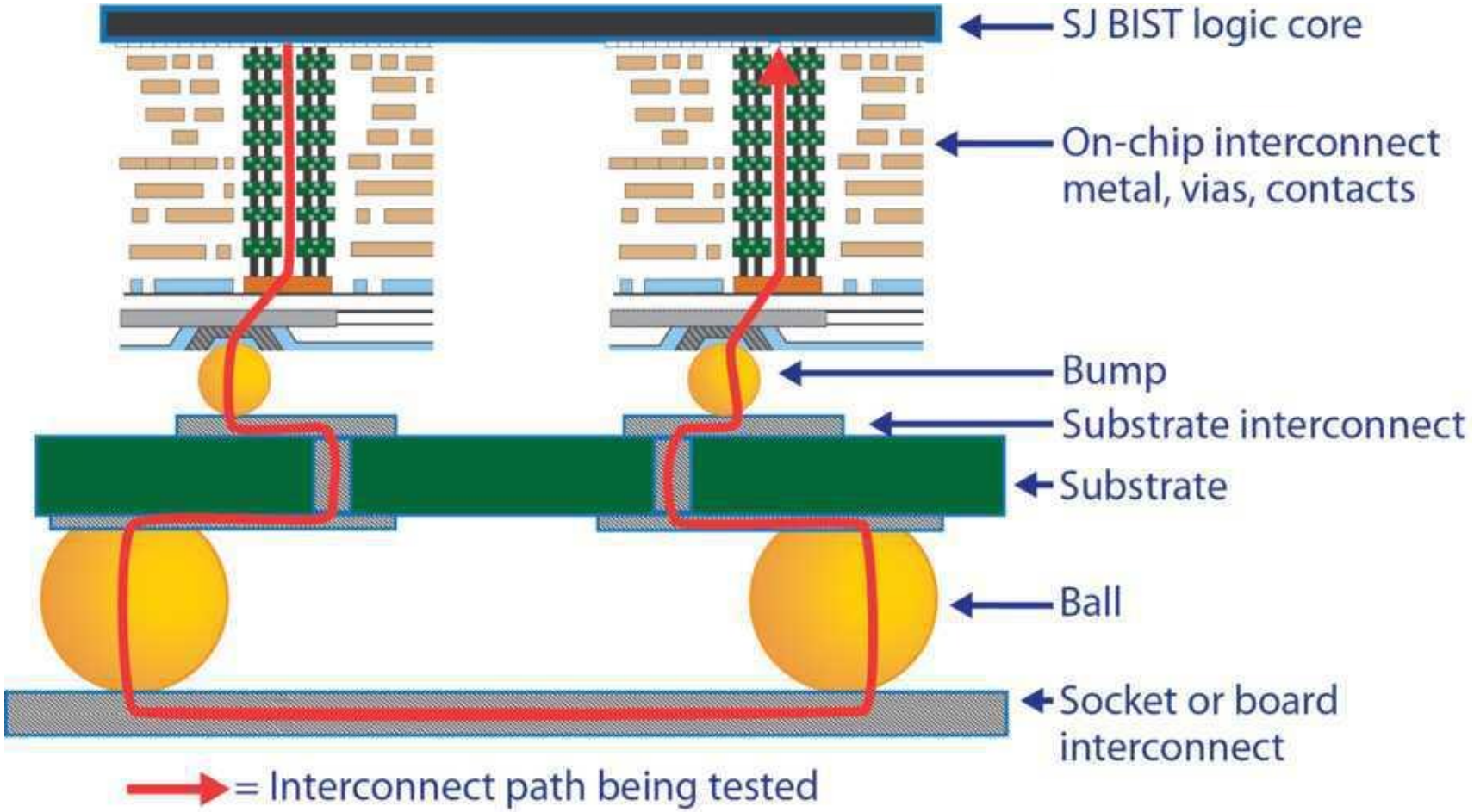
SJ BIST Application

Testing Die to Board



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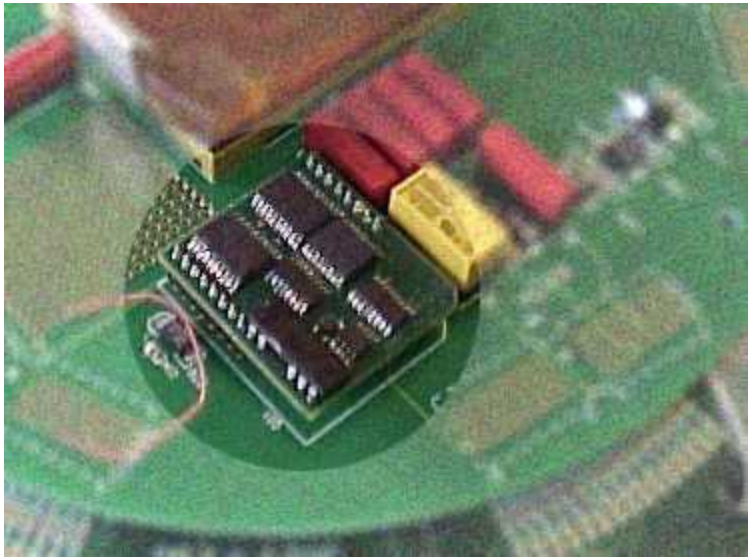
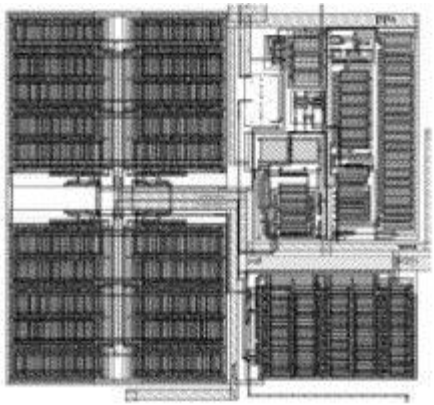
Precision Current Measurement : Q-Star Test

- I_{DDQ} ,I_{DDT}, I_{SSQ} and other precision current measurement instruments for characterization and test
- On-board modules and on-chip sensors
- Close to 1000 instruments being used on production test floors worldwide
- Developed by Ridgetop Europe
- Supported by Test and DFT consulting and training services





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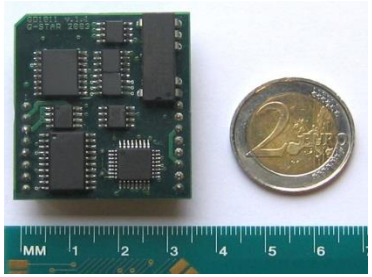
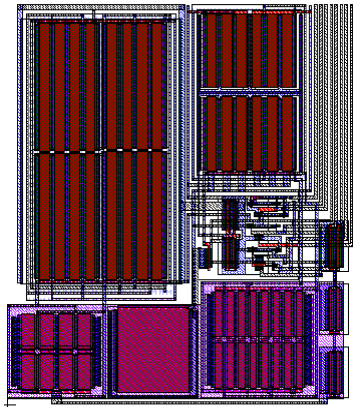
Precision Current Measurements

- Q-Star Test current monitors
  - Modules
    - → Packaged part testing, lab characterization, failure analysis
    - → I_{DDQ}, I_{DDT}, I_{SSQ}, power profiling, etc.
  - On-chip monitors
    - → PG-Mon: validates power, ground and other connections
    - → T-Mon: monitors transient currents



Q-Star QD-1011 monitor



Q-Star PG-Mon

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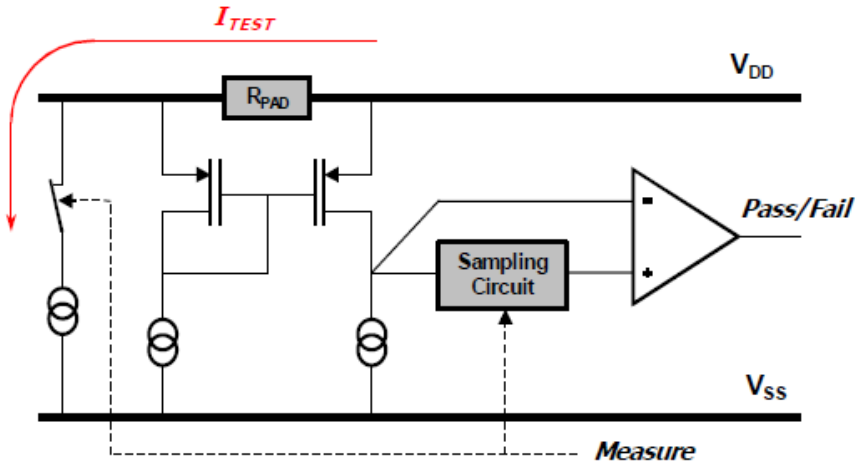
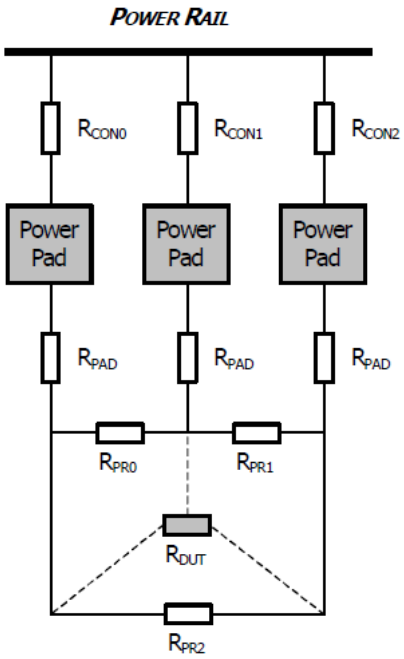
PG-Mon Application

- On-chip I/O and power/ground connection verification
- Highly sensitive (1.5 - 4Ω), non-intrusive observation of signals



Example:

VDD Monitor Block Schematic



Example:

IC Power Distribution Network Reliability Monitoring

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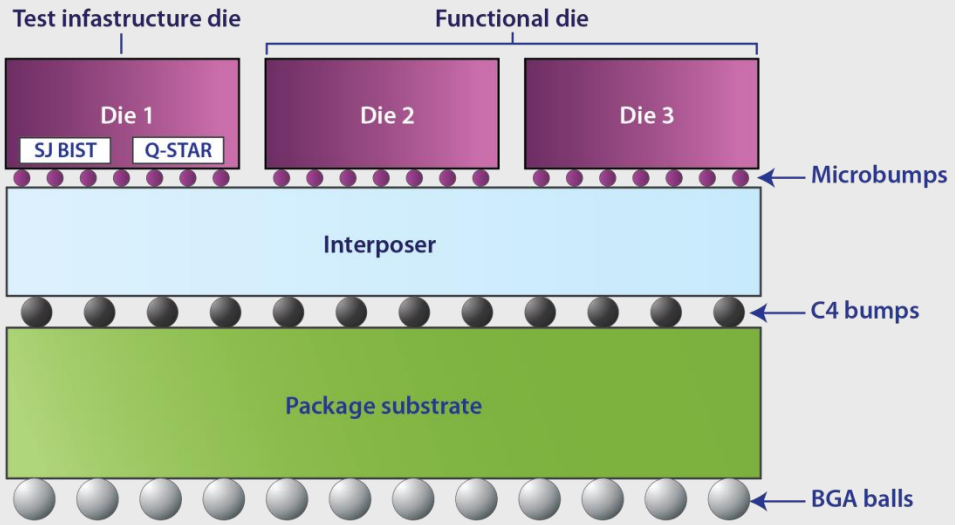
2.5D IC Reliability: Test Infrastructure Die

- "Test Infrastructure" die: Connects to strategic traces routed through the interposer
  - Most critical functionality
  - Most sensitive to degradation (e.g., corners or centers of Die 2 or Die 3)
  - Can monitor many signals
- SJ BIST/Q-Star IP embedded in Test Infrastructure die
- Advantages
  - Minimizes interposer overhead
  - Low cost IC
  - Upgrades are simple
- Disadvantages
  - Extra interposer real estate
  - Distance from some signals



2.5D IC Reliability: SJ BIST & Q-Star monitors embedded in a Test Infrastructure Die

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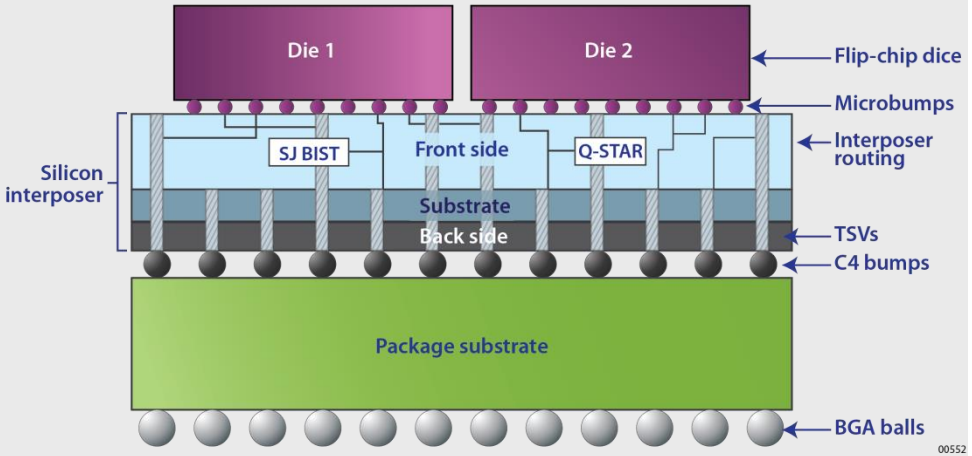
2.5D IC Reliability: Interposer-hosted

- Directly hosted on Interposer: Connects to strategic traces routed through the interposer
  - Most critical functionality
  - Most sensitive to degradation (e.g., corners or centers of Die 2 or Die 3)
  - Can monitor many signals
- SJ BIST/Q-Star IP embedded in Silicon Interposer
- Advantages
  - Minimizes interposer overhead
  - Monitors near key signals
- Disadvantages
  - Interposer cost is higher
  - Signal routing may be trickier



2.5D IC Reliability: SJ BIST & Q-Star monitors embedded in Silicon Interposer

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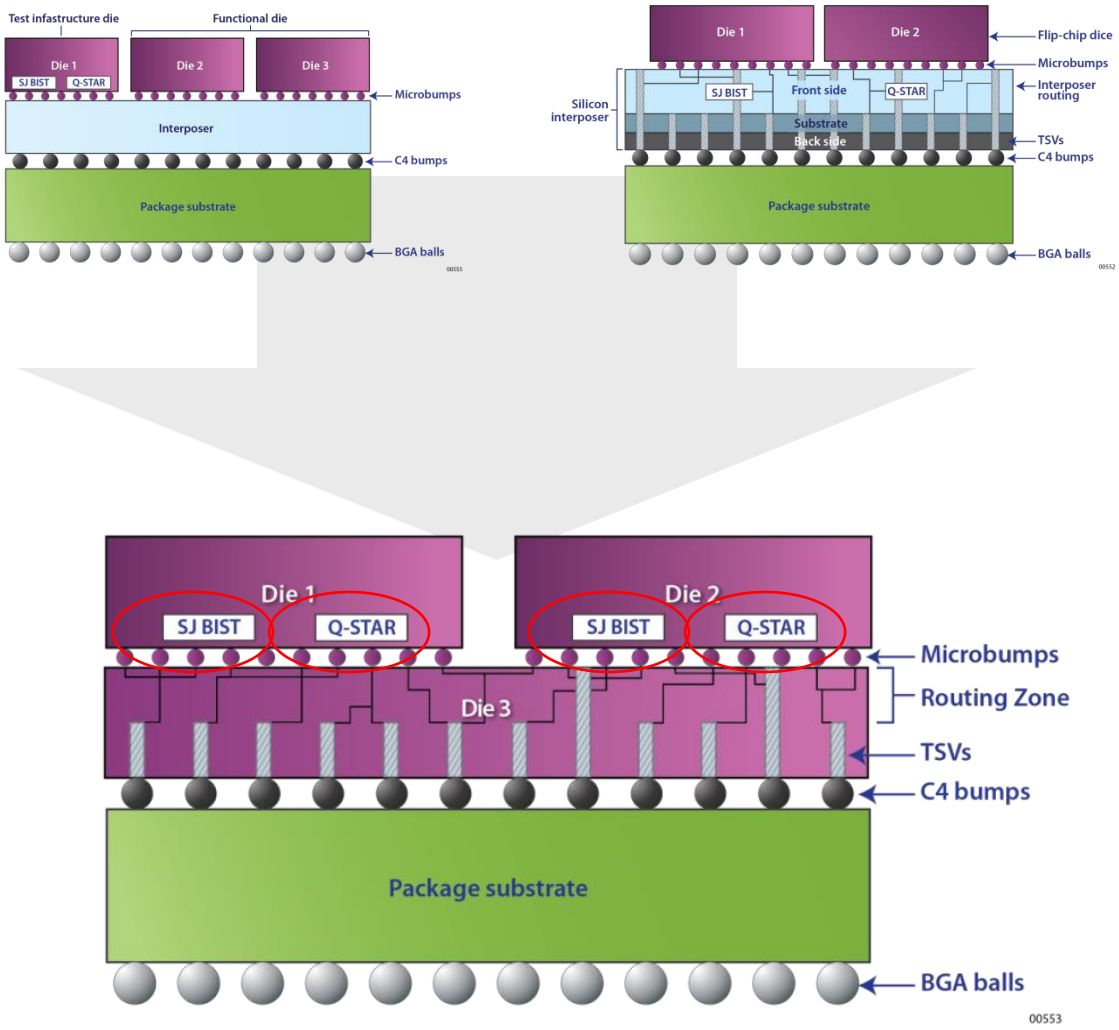
From 2.5D IC to 3D IC Reliability Monitoring



- 3D IC migration: Embed SJ BIST / PG-Mon IP in TSV-enabled ICs
- Required when no interposer present Highest quality monitoring
- Reduces cost and overhead
- Standardized approach for broadest applicability

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Summary

- 2.5D / 3D IC technologies pose new challenges
- Reliability assurance requires more than traditional test
- Real-time TSV BIST monitors…
  - Detect intermittencies
  - Identify degradation before failure
  - Are non-intrusive

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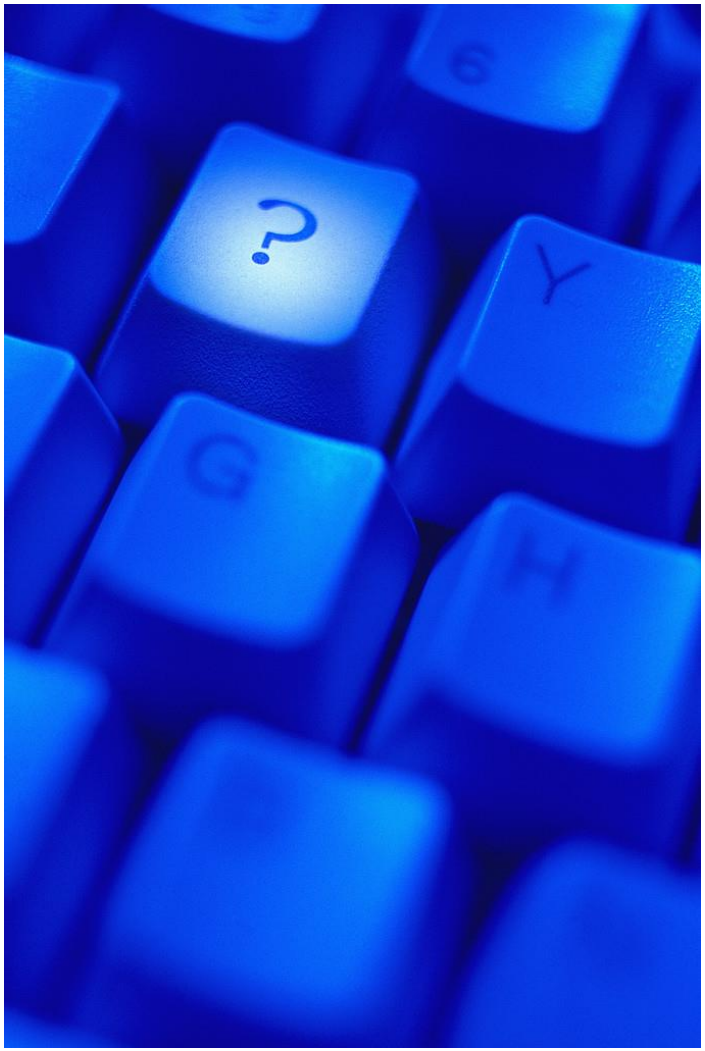

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- Slides and recording of the webinar will be available shortly via an e-mail from Ridgetop

- E-mail follow-up questions & comments to hans.manhaeve@ridgetop.eu

- Please fill out our brief feedback survey at https://www.surveymonkey.com/r/7KXDW6L

Thanks for your time and interest!

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