Contemporary Design for Testability
Guidelines for Circuit Boards and Systems

Louis Y. Ungar
President
Advanced Test Engineering Solutions

Andrew Levy
Vice President, Business Development
Ridgetop Group

December 10, 2014
Contemporary Design for Testability Guidelines for Circuit Boards and Systems

Presented by: Louis Y. Ungar
Sponsored by Ridgetop Group Inc., December 10, 2014

Copyright, 2014 by:
A.T.E. Solutions, Inc. Phone: (310) 822-5231 email: LouisUngar@ieee.org Web: www.BestTest.com
About the Presenter and Advanced Test Engineering (A.T.E.) Solutions, Inc.

Position – President of A.T.E. Solutions, Inc., the leading testability consulting and educational firm

Professional Associations – President of the Testability Management Action Group (TMAG), Consultant to the American Society of Test Engineers (ASTE), SMTA Testability Committee, Member of the IEEE and IEEE Standards Balloting Committee for IEEE-1149.1-2013 & IEEE-1687.

Major Accomplishments – Educated nearly 10,000 test professionals from 2 dozen countries, consulted more than 100 organizations, created BestTest information source for test professionals, patents for Built-In Self Test, worked on DFT standards for SMTA, IEEE, IPC. Created The Test Flow Simulator and The Testability Director, software packages…

Education – BS in Electronics Engineering and Computer Sciences from UCLA, completed course work for MA in Management

Professional Goals – Convince engineers and managers that product quality through better test is not only noble, but also cost-effective
Webinar Content

- What is DFT and Why We Need It?
- Guidelines and Standards for DFT and BIT
  - Military standards and guidelines
  - IEEE standards for boundary scan (JTAG)
  - Professional Society Guidelines
  - Commercial Company Guidelines
- New standards and guidelines
- New and coming technologies and solutions
WHAT IS DESIGN FOR TESTABILITY?

- Design for Testability is a philosophy incorporated in the design of electronic circuits which takes into consideration the post-design testing phase, and which attempts to reduce the effort and cost of testing.

Testability = Controllability + Observability
MOTIVATIONS FOR TESTABLE DESIGNS

- Reduce Test And Support Costs
- Gain Higher Product Quality Through Better Test
- Test Earlier And Improve Time To Market
Test Programming
The Greatest Cost of Test

Functional Test Programming

- Percent Fault Detection

- Without DFT
- With DFT
- With BIST

Engineering Effort, Time, Cost

95%
90%

Copyright, 2014 by:
A.T.E. Solutions, Inc. Phone: (310) 822-5231 email: LouisUngar@ieee.org Web: www.BestTest.com
The Most Important Testability Guidelines: When DFT Analysis is Performed and by Whom?

- **When?**
  - At conceptual design stage
  - During preliminary design stage
    » Block diagram
  - Several times during detailed design and before design release

- **Who?**
  - DFT Analysis can be performed by designers, test engineers and testability engineers.
  - Trade-off analyses between various options should involve management.
  - Actual design changes must be made by designers
DFT Guidelines and Standards
Design for Testability Guidelines and Standards

- Military Standards, Guidelines and Handbook
- IEEE Standards with Boundary Scan
- SMTA/TMAG Testability Guidelines
  Including probing and fixturing guidelines as well as “inspectability” for Automatic Optical Inspection and X-ray
- Commercial Guidelines
  For sale software and free guidelines from tool makers
- IPC Design for Excellence (DFX) Guidelines
- Emerging and Future Efforts
Military Standards, Guidelines and Handbook

FMECA - Procedures for Performing a Failure Mode Effects and Criticality Analysis MIL-STD-1629A Nov 1980


IEEE Standards with Boundary Scan

SMTA/TMAG Testability Guidelines

Commercial Guidelines

IPC Design for Excellence Guidelines

Emerging and Future Efforts
FMEA is a great input to DFT – Due early in design

FMEA provides important bases for Testability

- The number of failure modes identified provides a scope of how large the test will be
- Each failure mode that has an effect implies detectability
  - No effect implies testability problem
- Multiple effects for a failure mode imply diagnosis issues
  - A single effect for a failure mode means perfect diagnosis

Reliability and failure rate information in FMEA provides reliability weighting for both fault detection and isolation

IT IS CRUCIAL THAT FMEA BE PERFORMED EARLY IN THE DESIGN!
Includes:

DEFINITIONS AND ACRONYMS
- to help communicate across disciplines
  » PER MIL-STD-1309C
  » Detail Requirements
  » Test Descriptions and integration

Task Selection – to manage DFT
  » Task 100- Program monitoring and control
  » Task 200- Design and Analysis
  » Task 300- Test and Evaluation

Appendix A - Testability program application guidance

Appendix B- Inherent Testability Assessment – criteria in question form
  » Weighting and scoring different guidelines by designers and test engineers

Appendix C - Glossary
Purpose
To identify best practices in management, design and test in order to improve the reliability of fielded Built-In-Test (BIT) capabilities

Scope of BIT
Provides "built in" monitoring, fault detection and isolation capabilities as integral features of the system design.
BIT uses internal system hardware and software to test the system or its subsystems.
It often uses internal microprocessors and self-test software to isolate failures.
It can be supplemented with embedded "expert system" technology that incorporates diagnostic logic into the prime system.
  » These supplemental capabilities should be used to address specific BIT deficiencies that cannot be effectively addressed via other means.
Design for Testability Guidelines and Standards

- Military Standards, Guidelines and Handbook
- **IEEE Standards with Boundary Scan**
  - 1149.1 Digital Boundary Scan
  - 1149.4 Mixed Signal Boundary Scan
  - 1149.5 System Level Boundary Scan - **Dropped**
  - 1149.6 Boundary Scan for Differential and AC Coupled Circuits
  - 1149.7 2-pin Boundary Scan and Bulk Data Transfer
  - 1500 Embedded Cores Accessed via Boundary Scan
  - 1532 Boundary Scan to program on-board programmable devices
  - 1581 Interconnects Boundary Scan with memory and provides protocol
  - 1687 Transports results of embedded test via Boundary Scan
- SMTA/TMAG Testability Guidelines
- Commercial Guidelines
- IPC Design for Excellence (DFX) Guidelines
- Emerging and Future Efforts

Copyright, 2014 by:
A.T.E. Solutions, Inc.  Phone: (310) 822-5231  email: LouisUngar@ieee.org  Web: www.BestTest.com
What is Boundary Scan?

Typical Boundary-Scan Cell
SI = Scan In
SO = Scan Out
PI = Parallel In
PO = Parallel Out
CONSTRUCTION OF THE 1149.1 TEST ACCESS PORT (TAP)

TDI - test data input
TDO - test data output
TCK - test clock
TMS - test mode select
TRST - test reset

Bypass Register
Device ID Register
User Register
Instruction Register
Output MUX

Copyright, 2014 by:
A.T.E. Solutions, Inc. Phone: (310) 822-5231 email: LouisUngar@ieee.org Web: www.BestTest.com
1149.1 Boundary Scan Operation

1149.1 features are described in IC vendor supplied Boundary Scan Description Language (BSDL)

EXTEST Instruction

SAMPLE Instruction

Cluster

Bidirectional SAMPLE & EXTEST
IC Level BIST Controlled by Boundary Scan

Source: Goepel JTAG/ Boundary Scan Tutorial
Board Level BIST with Boundary Scan
IEEE 1149.4 - Mixed Signal Boundary Scan

- Approved as a full standard in 2001.
- Maintains the 1149.1 protocols, only adds analog capability.
- Still not in use…
Approved in 2003, it extends interconnect test to AC-coupled networks by providing:
- Differential interconnections
- AC coupled networks

 Defines hardware structure and two new instructions:
- The EXTEST_PULSE
- The EXTEST_TRAIN

Well supported and widely used

Source: Heiko Ehrenberg Goepel USA
IEEE-1149.7 Reduced-pin and Enhanced-functionality Test Access Port and Boundary Scan Architecture

**Benefits:**

Reducing the number of pins

» Only 2 pins needed for the TAP instead of 4 (or 5)

Improved support for devices with multiple cores

Increased debug performance

**Major Features (besides lower pin count)**

Advanced power management features

Star topology

Chip level bypass and Individual device addressing
1149.7 Star Topology and Chip-Level Bypass

Star Topology

Reduced Pin Count with 1149.7 Star-2 Topology:

Source: Corelis

Copyright, 2014 by: A.T.E. Solutions, Inc. Phone: (310) 822-5231 email: LouisUngar@ieee.org Web: www.BestTest.com
IEEE-1149.8.1 Boundary Scan Based Stimuli of Interconnections to Passive and/or Active Components

- **Traditional Vectorless Test** (Capacitive Opens Testing)
- **Using IEEE 1149.8.1 Boundary Scan Stimuli**
  - Standard released in 2012

---

**Sense plate**

**Buffer**

**Signal** (to Tester)

---

Tester AC Source stimulates one pin, all others are grounded

---

Drivers held constant

Stimulus waveform, derived from TCK and selectively applied to one driver.

---

Boundary Scan IC elsewhere on board with connectivity to the vacant connector.

---

Source: SMTA/TMAG Testability Guidelines TP101E, 2014
Approved in 2005, the IEEE-1500 hardware architecture comprises

- Instruction Register
- Wrapper Instruction Register and two data registers
- Wrapper Bypass Register (WBY)
- Wrapper Boundary Register (WBR).

» The use of Core Data Registers (CDRs) is also anticipated by the standard.
Design for Testability Guidelines

Copyright, 2014 by:
A.T.E. Solutions, Inc. Phone: (310) 822-5231 email: LouisUngar@ieee.org Web: www.BestTest.com
IEEE 1532-2002
In-System Configuration of Programmable Devices Standard

Copyright, 2014 by:
A.T.E. Solutions, Inc. Phone: (310) 822-5231 email: LouisUngar@ieee.org Web: www.BestTest.com
IEEE-1581 Static Component Interconnect Test Protocol and Architecture

- Approved in March 2011 it provides a means for a standard test methodology for memory interconnect testing.
- Describes test circuitry to be implemented in a memory device that bypasses the memory block itself and instead provides a logic connection between input and output pins (using simple logic gates).
- By stimulating the memory input pins and observing its output pins via boundary scan devices connected to the memory, board level connectivity can be verified.
IEEE-1687 Architecture

From: Asset Intertech White Paper, 2013

- Internal JTAG (IJTAG) Standard for Embedded Instruments became a standard in 2014. Includes
  - A chip’s boundary-scan TAP controller,
  - The device’s internal IJTAG scan path network
  - Portable interface for the embedded instrument.

  **Segment Insertion Bit (SIB)**
  - Acts as a gate
  - Allows on-demand access to instrument interface registers

---

Design for Testability Guidelines- 31 12/10/2014

Copyright, 2014 by:
A.T.E. Solutions, Inc.  Phone: (310) 822-5231  email: LouisUngar@ieee.org  Web: www.BestTest.com
Benefits from IEEE-1687

- **Allow test reuse**
  - IC level test run at board and system levels
  - Reduce test development costs to a single source

- **Improve diagnostics**
  - Reduce cost of diagnosis
  - Improve fault localization

- **Improve repair management**
  - Deep diagnoses available in the field, but repair is done in the factory
Military Standards, Guidelines and Handbook

IEEE Standards with Boundary Scan

SMTA/TMAG Testability Guidelines

- Probing and Fixturing
- Flying Probe
- Vectorless Test and IEEE-1149.8.1
- Automatic Optical Inspection (AOI) and X-ray (AXI)
- Electrical (Ad hoc DFT rules)
- Analog, Boundary Scan, BIST and System Level Diagnoses

IPC Design for Excellence (DFX) Guidelines

Commercial Guidelines

Emerging and Future Efforts
# Test Pad Positioning

![Diagram of test pad positioning](image)

## Table: Minimum Desirable Test Pad Positioning

<table>
<thead>
<tr>
<th>Priority</th>
<th>Target Size</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.035”</td>
<td>Provides most ideal target size.</td>
</tr>
<tr>
<td>2</td>
<td>0.035” top 0.030 bottom</td>
<td>Provides an acceptable target size when proper tooling holes are available.</td>
</tr>
<tr>
<td>3</td>
<td>Less than 0.030”</td>
<td>Can be used but contact repeatability will be sacrificed. Test fixture will require probe guide increasing cost.</td>
</tr>
</tbody>
</table>

*Source: SMTA/TMAG Testability Guidelines TP-101E*
Flying Probe Testers

- Flying probe testers can reliably hit test points with 0.025 in (0.64mm) diameters with 0.025 in. spacing.
  - Test vias and pads should be at least 0.014 in and have a 0.014 in free area, and should be accessible from one side of the board.
- Avoid probing large via holes
- Select the appropriate probe tip style
- Use board support to prevent flexing
- Optimize flying probe test times
  - e.g. Provide fixed access to large pin count nodes, such as ground and power nodes, on the PC board.

Source: SMTA/TMAG Testability Guidelines TP-101E
• Provides 18 “Design for Inspectability” Guidelines
• The combination of lighting and camera access requirements suggest an ideal 65-degree angle from vertical of unobstructed space.
• A minimum of 35 degrees is recommended when the full 65 degrees cannot be achieved.
Minimize overlapping solder joints on double sided boards

**Cross-Section**

Automatic X-ray Inspection (AXI)

**Manual X-ray (MXI)**

Uses Transmission X-ray

Source: SMTA/TMAG Testability Guidelines TP-101E
Design for Testability Guidelines and Standards

- Military Standards, Guidelines and Handbook
- IEEE Standards with Boundary Scan
- SMTA/TMAG Testability Guidelines

- Commercial Guidelines - (Several at IC level)
  - IC Level - About a half dozen scan, DFT and ATPG vendors
  - Boundary Scan – About a dozen Boundary Scan tool makers
  - General Board Level - ASTER’s TestWay, others?
  - System Level - DSI’s eXpress, QSI’s TEAMS, others?

A.T.E. Solutions’ The Testability Director™ includes hundreds of guidelines for ICs, Boards, Boundary Scan, System, Analog, BIST, etc.

- IPC Design for Excellence (DFX) Guidelines
- Emerging and Future Efforts
### Overall Worksheet

- **Title Sheet**
- **User's Guide**
- **Section Titles**
- **Section Weight Assignment**
- **Overall Testability Score**

#### Design for Testability Guidelines

<table>
<thead>
<tr>
<th>Section Title</th>
<th>Assigned Section Weight</th>
<th>Section Score in Percent</th>
<th>Section Weight</th>
<th>Section Weighted Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Guidelines</td>
<td>10</td>
<td>34%</td>
<td>1550</td>
<td>359.2</td>
</tr>
<tr>
<td>IC and ASIC Level Testability Guidelines</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VLSI, ASIC and Microprocessor Circuit Guidelines</td>
<td>6</td>
<td>60%</td>
<td>1380</td>
<td>1008.1</td>
</tr>
<tr>
<td>Memory and Programmable Circuit Guidelines</td>
<td>6</td>
<td>65%</td>
<td>450</td>
<td>303.5</td>
</tr>
<tr>
<td>8000000 Structural Device for Testability Guidelines</td>
<td>9</td>
<td>62%</td>
<td>452</td>
<td>280.2</td>
</tr>
<tr>
<td>B000000 Board Level Testability Guidelines</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inspection</td>
<td>6</td>
<td>78%</td>
<td>480</td>
<td>373.7</td>
</tr>
<tr>
<td>Automatic Optical Inspection Guidelines</td>
<td>6</td>
<td>84%</td>
<td>424</td>
<td>349.3</td>
</tr>
<tr>
<td>Automated X-Ray Guidelines</td>
<td>6</td>
<td>88%</td>
<td>424</td>
<td>361.3</td>
</tr>
<tr>
<td>Connectivity Guidelines</td>
<td>6</td>
<td>88%</td>
<td>424</td>
<td>361.3</td>
</tr>
<tr>
<td>Flying Probe Connectivity Guidelines</td>
<td>7</td>
<td>81%</td>
<td>560</td>
<td>451.8</td>
</tr>
<tr>
<td>Vectorless Test Guidelines</td>
<td>8</td>
<td>82%</td>
<td>560</td>
<td>451.8</td>
</tr>
<tr>
<td>Boundary-Scan Connectivity Guidelines</td>
<td>8</td>
<td>88%</td>
<td>560</td>
<td>492.8</td>
</tr>
<tr>
<td>In-Circuit Board Testability Guidelines</td>
<td>8</td>
<td>88%</td>
<td>560</td>
<td>492.8</td>
</tr>
<tr>
<td>In-Circuit Testability Guidelines</td>
<td>8</td>
<td>88%</td>
<td>560</td>
<td>492.8</td>
</tr>
<tr>
<td>Boundary-Scan In-Circuit Testability Guidelines</td>
<td>8</td>
<td>88%</td>
<td>560</td>
<td>492.8</td>
</tr>
<tr>
<td>Functional Board Test and Testability Guidelines</td>
<td>8</td>
<td>88%</td>
<td>560</td>
<td>492.8</td>
</tr>
<tr>
<td>Digital Circuit Guidelines</td>
<td>7</td>
<td>93%</td>
<td>1470</td>
<td>1386.7</td>
</tr>
<tr>
<td>Analog Circuit Guidelines</td>
<td>8</td>
<td>91%</td>
<td>1470</td>
<td>1343.3</td>
</tr>
<tr>
<td>Board Level Boundary-Scan and BIT Guidelines</td>
<td>8</td>
<td>85%</td>
<td>1530</td>
<td>1295.2</td>
</tr>
<tr>
<td>System Level Testability Guidelines</td>
<td>8</td>
<td>65%</td>
<td>1120</td>
<td>738.0</td>
</tr>
<tr>
<td>General System Level Guidelines</td>
<td>8</td>
<td>83%</td>
<td>1120</td>
<td>931.7</td>
</tr>
<tr>
<td>System Level BIT Guidelines</td>
<td>8</td>
<td>83%</td>
<td>1120</td>
<td>931.7</td>
</tr>
<tr>
<td>Totals</td>
<td>64</td>
<td>64%</td>
<td>6400</td>
<td>3984</td>
</tr>
<tr>
<td>Overall Testability Score</td>
<td>64</td>
<td>64%</td>
<td>6400</td>
<td>3984</td>
</tr>
</tbody>
</table>

Copyright, 2014 by: A.T.E. Solutions, Inc. Phone: (310) 822-5231 email: LouisUngar@ieee.org Web: www.BestTest.com
### Where to Improve Testability

http://www.besttest.com/OurProducts/TestabilityDirector/

---

**The Testability Director**

<table>
<thead>
<tr>
<th>Section</th>
<th>Assigned Weight</th>
<th>Section Score in Percent</th>
<th>Weighted Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>G00000</td>
<td>10</td>
<td>34%</td>
<td>720.0</td>
</tr>
<tr>
<td>B10000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B11000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B13000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B50000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B51000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B53000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B70000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B71000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B73000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B75000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S00000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S01000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S03000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Overall Testability Score</strong></td>
<td></td>
<td></td>
<td>80%</td>
</tr>
</tbody>
</table>

**Needs to Improve!**
### General and Management Guidelines

#### Criteria Weight
- Assigned by Test

#### Criteria scoring
- Determined by designers

#### Find specific items to improve!

### Table

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Total</th>
<th>Meeting</th>
<th>Score</th>
<th>Weighted Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Guidelines</td>
<td>100</td>
<td>100</td>
<td>75%</td>
<td>45.0</td>
</tr>
<tr>
<td>Are design requirements and specifications clearly documented prior to the start of any design implementation?</td>
<td>9</td>
<td>10</td>
<td>3</td>
<td>30%</td>
</tr>
<tr>
<td>Are DFT assessments made a part of design reviews at the beginning of conceptual, block diagram, and circuit design stages?</td>
<td>9</td>
<td>15</td>
<td>10</td>
<td>67%</td>
</tr>
<tr>
<td>Is the entire development team aware of testability requirements?</td>
<td>8</td>
<td>5</td>
<td>2</td>
<td>40%</td>
</tr>
<tr>
<td>Is a Failure Mode Effects (Criticality) Analysis being performed for each design milestone?</td>
<td>9</td>
<td>15</td>
<td>10</td>
<td>67%</td>
</tr>
<tr>
<td>Are the test strategy and DFT interactively traded-off during the design process?</td>
<td>6</td>
<td>100</td>
<td>75</td>
<td>75%</td>
</tr>
<tr>
<td>Is the test equipment and tester software to be used selected?</td>
<td>4</td>
<td>5</td>
<td></td>
<td>20%</td>
</tr>
<tr>
<td>Is testability review a part of the design review?</td>
<td>10</td>
<td>3</td>
<td>1</td>
<td>67%</td>
</tr>
<tr>
<td>Has a Level of Repair Analysis been accomplished?</td>
<td>7</td>
<td>8</td>
<td></td>
<td>25%</td>
</tr>
<tr>
<td>For each maintenance level, has a decision been made for each item on how built-in test (BIT), automatic test equipment (ATE), and general purpose test equipment will support fault detection and fault isolation?</td>
<td>9</td>
<td>100</td>
<td>10</td>
<td>10%</td>
</tr>
<tr>
<td>Is the planned degree of test automation consistent with the capabilities of the maintenance technician?</td>
<td>9</td>
<td>100</td>
<td>10</td>
<td>10%</td>
</tr>
<tr>
<td>Have testability objectives been determined?</td>
<td>8</td>
<td>100</td>
<td>10</td>
<td>10%</td>
</tr>
<tr>
<td>Have restrictions been established in meeting testability objectives?</td>
<td>9</td>
<td>100</td>
<td>10</td>
<td>10%</td>
</tr>
</tbody>
</table>

#### Section Totals
- 105
- 34%
- 359.2
Design for Testability Guidelines and Standards

- Military Standards, Guidelines and Handbook
- IEEE Standards with Boundary Scan
- SMTA/TMAG Testability Guidelines
- Commercial Guidelines
- **IPC Design for Excellence (DFX) Guidelines**
- Emerging and Future Efforts
Work in progress, expected release Feb 2015 at APEX conference

Encompasses

» Design,
» Validation,
» Manufacturability,
» Reliability,
» Supportability… and

Design for Testability
<table>
<thead>
<tr>
<th>Development Phase</th>
<th>Design Activity</th>
<th>Testability Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conceptual Design</td>
<td>Create product specifications</td>
<td>Create test requirements for each product specification, including fault detection, diagnosis, test times, test costs, etc.</td>
</tr>
<tr>
<td>Block Diagram</td>
<td>Define partitions between blocks</td>
<td>Ensure that all partitions are controllable and observable to all inspection and test equipment considered. The mix of inspection and test equipment stages should be determined and test resources identified and procured.</td>
</tr>
<tr>
<td>Detailed Circuit Design</td>
<td>Electrical design of printed circuit boards (PCBs), including identification and procurement of parts. Trade-off in components.</td>
<td>Ensure that parts with built-in test, such as boundary scan are given preference. Ensure that controllability and observability within the circuit are maintained. Ensure that “inspectability” for AOI and X-ray is considered. Ensure that bed-of-nails, flying probe or boundary scan access to all signals is available. All test program development can start here.</td>
</tr>
<tr>
<td>Circuit Design Verification</td>
<td>Ensure circuit performs functions specified within tolerances and accuracies specified</td>
<td>Create and run design verification tests using discrete instruments or ATE. (Note ATE is not necessary as test should only run once and the design verification test is different manufacturing tests. The former looks for design errors, the latter for defects. In some cases manufacturing tests can also be used for field support tests.) Environmental stress screening (ESS) such as HALT and HASS should be performed here. To enable this, the product must be testable.</td>
</tr>
<tr>
<td>Manufacturing</td>
<td>PCB Layout</td>
<td>Circuit board accessibility issues need to be addressed to ensure sufficient access by the inspection and test equipment used in production.</td>
</tr>
<tr>
<td>Support</td>
<td>Field support and factory returns</td>
<td>Ensure that tests developed for systems accurately identify failing subsystems or parts that can be replaced quickly and easily by end user. While manufacturing tests can be utilized once the product is returned to the factory, field support tests typically utilize built-in test (BIT or BIST) to repair by replacement. Design for BIT must take place as early as the Block Diagram phase.</td>
</tr>
<tr>
<td>Prognosis</td>
<td>Product Health Management</td>
<td>Ensure (during the Detailed Circuit Design phase) that there are sufficient monitoring points and mechanisms to ensure that (life critical) product degradations can be detected and diagnosed.</td>
</tr>
</tbody>
</table>
Design for Testability Guidelines and Standards

- Military Standards, Guidelines and Handbook
- IEEE Standards with Boundary Scan
- SMTA/TMAG Testability Guidelines
- Commercial Guidelines
- IPC Design for Excellence (DFX) Guidelines

**Emerging and Future Efforts**

System Level – SJTAG
DFT in 2020
SJTAG and System Level Boundary Scan Chain

SJTAG

Standardize data contents and formats for communication:

» between external Test Manager platforms and internal Embedded Test Controllers

■ eXternal Boundary Scan Test (XBST)

and

» between Embedded Test Controllers and the UUTs they serve

■ Embedded Boundary Scan Test (EBST)
How will DFT change by 2020?

- **Topics that will likely impact the future**
  - IDDQ Testing of CMOS (boards and systems)
  - SJ BIST from Ridgetop Group - Andrew Levy will cover this next
  - Thermal Imaging for Diagnoses
  - Prognostic Health Management for all electronics
  - No Fault Found (NFF) and False Alarms > 70% of repairs
  - Overcome DFT & BIST security threats
  - Built-In Self Repair and Built-In Self Healing

- **We’ll keep you informed through our courses.**
  [http://www.besttest.com/Courses/](http://www.besttest.com/Courses/)

- **We’ll keep The Testability Director updated!**
  [http://www.besttest.com/OurProducts/TestabilityDirector/](http://www.besttest.com/OurProducts/TestabilityDirector/)
Existing Test Methods

- Focus on Manufacturing Process
  - Boundary Scan (JTAG / IEEE 1149.1)
  - Optical / X-Ray Inspection
- Focus on Static Measurements
- Reliability Measurements Are Lacking
  - Reliability = Performance over Time
  - Implies field measurement & monitoring
  - Intermittencies develop after deployment
An interconnect intermittent fault is an event that causes the interconnect resistance to increase for a predefined amount and last for a minimum time.

Fault detection is linked to # of occurrences

Definition evolved:
- From: R increase of $1K\Omega$ lasting at least $1\mu s$
  \[ \rightarrow \text{JEDEC 22-B111} \]
- To: R increase of $200\Omega$ lasting at least $200\text{ns}$

Interconnect is classified as failing if subsequent to the occurrence of the first event, nine more events are detected that occur within a period of time $T_2$ that is less than or equal to 10% of the time to the occurrence of the first event $T_1$. ($T_2 \leq 0.1*T_1$)
With present technology, reported electronic system problems in the field cannot be duplicated at the service point or in the lab

“Three/Four-letter” words (CND, NTF, RTOK)
- Could Not Duplicate (CND)
- No Trouble Found (NTF)
- Retest OK (RTOK)

50 to 80% of these CND/NTF/RTOK problem categories are reported by service personnel.

Major culprits – Solder joint intermittencies and NBTI effects in deep submicron ICs
Defects: Fractures & Intermittency

High Stress Areas

FPGA Die Outline


Failure Point: Fracture of the Solder Ball

Intermittent Failure caused by Fractured Solder Joint and Vibrational Stress

BGA Package
Fracture
Solder Ball
Multi-Layer PCB
Layer 1
Layer 2
Layer 3
Contact Pad
PCB Land
Dielectric

Open Circuit
Closed Circuit
SJ BIST™

- SJ BIST = Solder Joint Built-in Self-Test
  - Verification & validation of solder joint interconnect reliability
    (Methodology applies any type of interconnection)

- Objectives
  - Detection of impending interconnect failures
  - Unique in-situ testing in operating circuits
  - Technology-independent

- Features and Benefits
  - Detects ball fractures prior to catastrophic failure of circuit
  - Provides actionable maintenance data
  - Independently tested and verified
  - Endorsed by leading automotive and aerospace customers
  - Also used for Highly Accelerated Life Test (HALT)
  - Complements standard manufacturing test methods
• Similar to a simple memory test: W0 – R0; W1 – R1
• Runs concurrently with host circuit
• Verilog/VHDL core (patent pending)
  • Each core tests two I/O pins
  • Pins are externally wired together
  • Optionally small capacitor connected to the two pins
About Ridgetop Group, Inc.

- Incorporated in 2000, and headquartered in Tucson, AZ. Ridgetop Europe established in 2010 in Belgium.

- Microelectronic Design and Test Solutions:
  - SJ BIST™ Based Test Solutions
  - ProChek™ Semiconductor Characterization System
  - Q-Star Test™ Precision Current Measurement Instruments
  - PDKChek™ In-Situ Test Structures
  - ISO:9001/AS9100C-compliant Design and Integration Services

- Strong market position with commercial and government customers in USA, Canada, Europe, and Asia
Questions?

- Slides and recording of the webinar will be available shortly via an e-mail from Ridgetop.

- E-mail follow-up questions & comments to:
  - Louis Ungar: louisungar@ieee.org
  - Andrew Levy: andrew.levy@ridgetopgroup.com

- Please fill out our brief feedback survey at: https://www.surveymonkey.com/s/RCFP27Y
Thank you!

Ridgetop Group, Inc.

3580 West Ina Road
Tucson, AZ 85741