How 3D Architecture and 2.5D Interconnect Change the World

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VP Marketing
Why 3D? – Expiring Economics

AMD 2014 3D-ASIP
Why 3D? – Power is killing us

DIE STACKING MOTIVATION (MEMORY INTEGRATION)

AMD 2014 3D-ASIP
Why 3D? – Apples & Oranges

AMD 2014 3D-ASIP
Conventional RAM Architecture

Memory Bits

Periphery
- Decoders
- Amps
- Drivers
- etc.
Conventional 3D Packaging

- Preserves traditional RAM problems
- Adds stacking costs
DiRAM™ True 3D RAM Architecture
Dis-Integrated 3D RAM Architecture

DiRAM™ Architecture

Memory Cells and Access Transistors

Sense Amps, etc.

I/O Layer
DiRAM4 64C64 Performance

- **64 Gb** Storage
- 64 Ports
- 128 Channels
- **4096** Banks
- **> 4** Terabit/s Data Bandwidth
- 9 ns Latency
- **64 Billion** Transactions Per Second (Minimum)

256 Independent RAMs
DiRAM4 Scale* Drawing

Top View
175 mm²

Side View
0.5 mm

Isometric View
87.5 mm³

* Almost to scale
Via-Free Wafer Stacking

Aggressive Copper TSV
≈ 5µ x 50µ

Tezzaron Tungsten SuperContact™
<1µ x <10µ
Common, Cheap, Fast and... Dense

5μ Diameter Copper TSVs (Stress driven Pitch)

<1μ Diameter Tungsten SuperContacts (Alignment driven Pitch)

Tezzaron wins: >66 to 1
Radically Different Manufacturing

Conventional Flow
• Fabricate Wafer
• Probe Test Die
• Thin Wafer
• Singulate Die
• Stack Good Die
• Package Stack
• Burn-In & Test Stack

Tezzaron Flow
• Fabricate Wafer
• Stack Wafers
• Thin Top Wafer
• Repeat
• Probe Test Stacks
• Singulate Stacks
• Package Stacks
• Burn-In & Test Stack
“That can’t work…”

“…bonding un-tested die will produce near zero yields, poor reliability and high costs.”

Translation

You Tezzaron people are crazy!
Super dense interconnect allows...

**Bi-STAR™**

**Built-in Self Test And Repair**

- Controlled by *embedded* ARM processor
- Enabled by *per-cell* control interconnect
- Super-fine grained test and repair
- Continuous, in-the-system hard and soft error repair
Bi-STAR Repair Improves Yield

Stack Height

Yield

100%
Solve 3D Problems with 3D

Bonding Untested Wafers

Enables Effective Repair

Enables Super Thin Wafers

Enables Tiny Vias
DiRAM: Efficiency for the Future

- Less aggressive wafers
- Higher array efficiency
- Much lower test cost
- Higher yield
- Longer product life cycles
1Tb/s Ayrees™ Memory Block

Integrated Configuration and Power

DiRAM4 ← Tagging Hub → DiRAM4

512 pin Low Voltage SyoPort™ Interface

Two 64 Gb DiRAM4 stacks
One Tagging Hub die
Integrated Configuration Management and Power Resources
High End Routing

Tasks

• Packet Buffer
  (Burst Read/Write)

• Tables
  (Read Dominated)

• Stats
  (Read-Mod-Write)

Performance Metrics

• Density
  – Line Rate / Seconds

• Bandwidth
  – Line Rate x 2.5

• Transaction Rate
  – Transactions x Line Rate / Min Packet Size
400Gb NP Standard RAM BOM

(30) 4 Gb DDR3 DRAMs = 1 Tb/s Packet Buffer

(12) 576 Mb RLDRAM3 DRAMs = 12 BT/s Tables

(4) 576 Mb SigmaQuad-Ille SRAMs = 5 BT/s Stats
400Gb Routing with DiRAM4

Network Processor
22 mm x 19 mm

DiRAM4
14 mm x 12.5 mm

26 mm x 32 mm Interposer
RAM is now Singular
DiRAM4™ Changes the Language of System Design…

DiRAM4™ in Networking
- High Transaction Rate
- High Bandwidth
- High Density

DiRAM4™ in Computing
- High Bandwidth
- High Density
- Small References

DiRAM4™ in Everything
- Multiple Independent Channels
- High Bandwidth
- High Transaction Rate

Network Processor
Tezzaron DiRAM4
Table Memory + Packet Buffer

High Performance Processor
Tezzaron DiRAM4
Local Memory and/or Cache

FPGA
Tezzaron DiRAM4
Fast Local Memory
Performance Choices

- I/O Die Integration – Full Stack Performance (16 to 32 Tb/s)
- I/O Die Interface (4 to 8 Tb/s)
- SyoPort™ Interface (1 Tb/s Duplex)
- "Std" Interface
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Novati Technologies - Austin

- Tezzaron subsidiary
  - Manufacturing volume
  - Services available
- 3D Assembly Options
  - Cu-Cu
  - DBI®, Oxide Bonding
  - Intermetallic
  - Gold-Indium, Gold-Gold
- Silicon Interposers
  - Passive
  - Passive Plus
  - Active
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