Ridgetop Group Inc
ENGINEERING INNOVATION

Solve Interconnect Reliability Issues Using Flip-Chip Testing with SJ BIST™

Ridgetop's SJ BIST provides you with a digital solution for ongoing monitoring of interconnection reliability in advanced flip-chip package types. You can use it at final package test in the factory to weed out faulty parts, or after the flip-chip package is deployed in the field to detect degrading connections and intermittent failures. The technology is also extensible to handle new 3D implementations and high-density connector applications.

Use of the flip-chip packaging technique continues to grow because of its advantages in size, flexibility, cost, and more. Flip-chips enable a larger number of interconnects in shorter distances than conventional wire-bond chips. However, interconnect reliability problems are commonly experienced when using large ball grid array (BGA) packages with embedded flip-chip devices. The reliability issues are primarily related to the on-chip interconnect in the following ways:

- stacked vias used in flip-chip-to-substrate interconnect (solder bumps)
- packaging/package assembly process
- package-to-board interconnect (to a lesser extent)

Ridgetop's SJ BIST is a small digital IP core embedded in the silicon that was originally developed to investigate and monitor solder joint reliability on BGA packages, but it is equally well-suited to investigate and evaluate various aspects of interconnect reliability.

SJ BIST gathers information on the reliability aspects of the interconnect chain as a whole (die-to-board interconnect involving on-chip interconnects; chip-to-substrate interconnect, i.e., solder bumps; and substrate-to-board interconnect, i.e., solder balls). It also gathers reliability information on sub-aspects of the die-to-board interconnect chain, such as the on-chip interconnect section and the chip-to-substrate interconnects involving the bumps.

SJ BIST makes its interconnect reliability observation by monitoring the amount of charge transferred over a given amount of time between its two observation terminals. It does this by writing out a sequence of 1's and 0's out of one of its observation terminals and verifying the arrival of the correct sequence at the other observation terminal, and vice versa. (Data are sent back and forth between the two terminals.) A small capacitor connected to the interconnect being observed defines the detection threshold as a function of the data transfer frequency being used. If the reliability of the observed interconnection is affected, causing either increased interconnect resistance or intermittent contact behavior, then this affects the charge transfers between the SJ BIST observation terminals, leading to a failure of the executed test.

SJ BIST runs stand-alone and can be used to observe the reliability of the interconnect path between its two observation terminals throughout the lifetime of the product in which it is embedded either in a sampled way (at dedicated timing points under control of the user) or continuously (free running mode). SJ BIST can provide diagnostics related to intermittent fault occurrences as well as pass/fail information

Different instantiations of SJ BIST allow reliability investigation of the following types of interconnect paths, as illustrated in Figure 1:

- on-chip interconnects (from one interconnect layer to another addressing contact, metal, and (stacked) via reliability)
- chip-to-substrate reliability (involving on-chip interconnect and chip-to-substrate bump reliability)
- chip-to-board interconnect reliability (involving on-chip interconnects, bumps, substrate and balls)

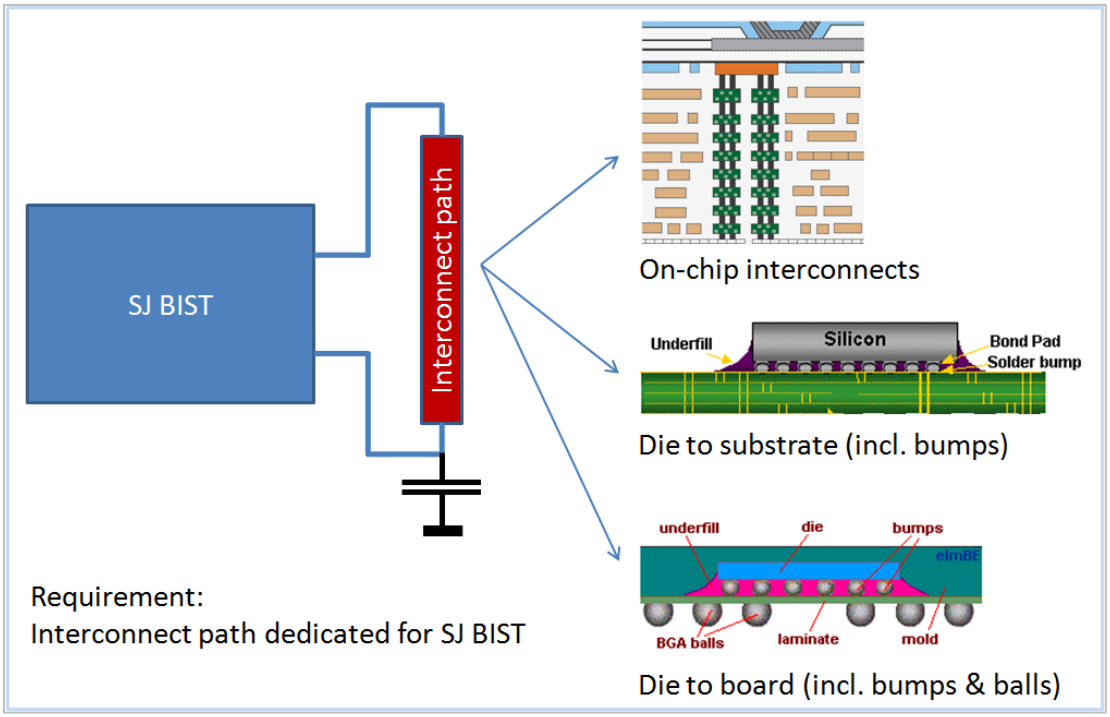

Figure 1: SJ BIST can detect on-chip, die-to-substrate, and die-to-board flip-chip interconnection problems

Support

Our experienced application engineers will help you configure a comprehensive and cost-effective testing solution.

Contact us today to find out how SJ BIST can help you solve interconnect reliability issues by calling +1 520-742-3300 or by email at info@ridgetopgroup.com.