## RGADC-14B-3G-RH

Comparison Ridgetop Group Inc

ΙΝΝΟΥΑΤΙΟΝ

## **PRODUCT BRIEF**

# Rad-Hard Programmable SiGe ADC, 3 GS/s at 12-bit, 500 MS/s at 14-bit Resolution

<u>N G I N E E R I N G</u>

InstaCell<sup>™</sup> Semiconductor IP

#### **Features and Benefits**

- Time-interleaved pipeline architecture
- 500 MS/s to 3 GS/s sampling speed
- 12-14 bits resolution, programmable (11-12 bits ENOB)
- SiGe BiCMOS technology
- Uses 77% less power than commercially available ADCs
- Two configurable pipeline channels
- Four programmable operation modes
- Hard to 1 Mrad TID
- Hard to 120 MeV-cm<sup>2</sup>/mg SEL

#### **General Description**

Ridgetop's radiation-hardened programmable SiGe analog-to-digital data converter (ADC) has fast digitization with extremely high linearity and dynamic range to achieve system performance targets. In many applications, with the added requirement of radiation hardness and low power, the ADC is a critical chokepoint that must meet demanding standards. Accordingly, Ridgetop's ADC is highly linear with an INL and DNL of no more than  $\pm 0.5$  LSB, an operating temperature range of at least -10 to 80 °C, a very high effective number of bits (ENOB) of 11.0, and a total ionizing dose (TID) rating of 1 Mrad. The ADC employs an innovative time-interleaved pipeline architecture and is based on the advanced silicon-germanium (SiGe) bipolar complementary metal oxide semiconductor (BiCMOS)

technology, providing an effective number of bits more than 2 bits higher (ENOB = 11.0 bits) than the best commercially available 3 GS/s ADC.

Additionally, the ADC conserves valuable power because it uses 77% less power than commercially available ADCs. For maximum flexibility, the ADC provides four configurable pipeline channels and two programmable operation modes: (1) 12-bit (ENOB = 11.0 bits), 3 GS/s, 860 mW; (2) 14-b (ENOB = 12.0 bits), 500 MS/s, 860 mW.



Ridgetop's time-interleaved ADC architecture; IP sub-blocks are also available

#### Specifications of RGADC-14B-3G-RH

PARAMETER	SPECIFICATION
Topology	Time-interleaved pipeline
Resolution	12-14 bits, programmable
Sampling speed	500 MS/s to 3 GS/s, programmable
Power consumption	<860 mW
Input analog bandwidth	6.4 GHz
Digital output data format	LVDS
Analog supply voltage	3.3 V
Digital supply voltage	2.5 V
Digital I/O supply voltage	1.2 V
Analog input voltage	1.2 V peak-to-peak (differential)
Input capacitance	5 pF
Input reference voltage	1.2 V (typ.)
Input voltage range	0.6 to 1.8 V
Temperature range	-10 to 85 degrees C
Latency (# clock cycles)	10
INL	<0.5 bit
DNL	<0.5 bit
Area	2.5 mm <sup>2</sup>
Process	SiGe BiCMOS
Foundry*	IBM 130 nm
Radiation hardness**	TID: 1 Mrad, SEL: 120 MeV-cm <sup>2</sup> /mg
THD	-74 dB
ENOB	11-12 bits
Power supply	4.5, 2.5 V
Power supply tolerance	±5%

# IP Sub-blocks Available With Separate License

- Extremely fast track-and-hold amplifier
- Ultra-fast op-amps
- Complete pipeline stages

## **Applications**

The full ADC and its constituent IP blocks can be used to achieve the highest level of performance in many applications including:

 Space-based microelectronics applications such as laser radar and satellite communication (SATCOM)

- Wireless LAN and wireless RF infrastructures
- Test and measurement instrumentation
- Data acquisition systems
- Software-defined radio
- Telecommunications receivers
- Automatic test equipment

\*May be ported to other foundries or nodes \*\*IP may also be available in non-rad-hard form



Ridgetop is AS9100C/ IS09001:2008 certified and has Trusted IC Design Supplier accreditation from U.S. Defense Microelectronics Activity (DMEA)

## Need modified or custom design? Contact Ridgetop at 520-742-3300 to discuss your ideal solution!

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