RGADC12B650MRH

PRODUCT BRIEF

Ridgetop Group Inc

ENGINEERING INNOVATION

12-bit, 650 MS/s, Rad-Hard SiGe ADC, IBM 130 nm IP Core

InstaCell™ Semiconductor IP

Innovative High-Performance, Radiation-Hardened ADC Technology

- 12 bits of resolution (11-bit ENOB)
- 650 MS/s sampling rate
- IBM 8HP 130 nm SiGe process
- 1.5 GHz analog bandwidth
- 650 mW power
- Hard to 300 krads (Si) of TID
- Hard to 120 MeV-cm^2/mg of SEL
- 2.5 V, 4.5 V analog supply voltage
- 1.2 V digital I/O supply voltage
- Input range 2 V
- Pipeline architecture

General Description

Ridgetop's rad-hard pipeline ADC is optimized for high performance applications that require very high input analog bandwidth and low power consumption, including spaceborne applications. This ADC is designed in the IBM 8HP silicon-germanium BICMOS process. The ADC has a full-speed, front-end sample-and-hold amplifier (SHA) that can accept input analog bandwidth to 1.5 GHz.

The ADC structure shown in Figure 1 is a 2-channel time-interleaved pipeline ADC with an input SHA. The sampling frequency of the SHA can be as low as 650 MHz to under-sample the input IF-signal of 1.5 GHz. After the IF signal is sampled with the SHA, two channels of pipeline ADCs digitize the base-band signal. The sample rate of each channel is half of the sample rate of the SHA.

Each pipeline channel consists of one 2.5-bit stage, eight 1.5-bit stages, and a 3-bit flash ADC at the end, which are available as building blocks for other ADCs. The sub-blocks include bandgap reference (BGR), three separate operational transconductance ampliers (OTAs), comparators, the ADC pipeline stages, and the SHA.

Applications

- Communication applications
- Satellite applications
- Medical imaging
- Software-defined radio
- Detectors
- Instrumentation

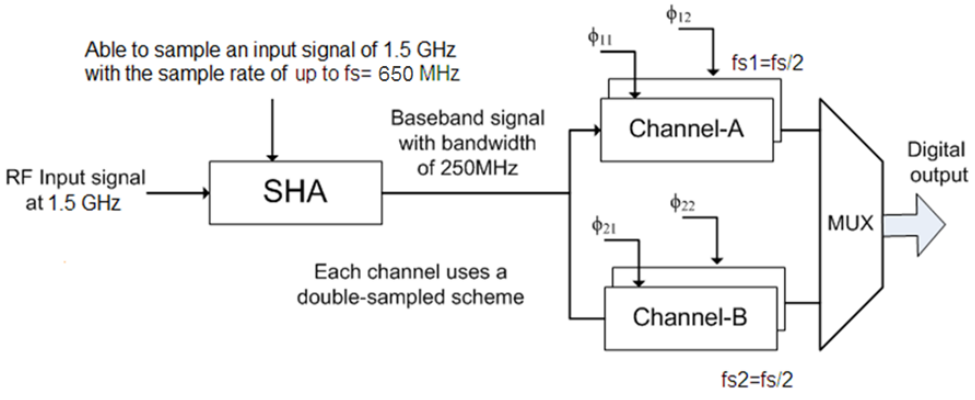

Figure 1: Time-interleaved pipeline ADC architecture; IP sub-blocks are also available

Table 1: Specifications of the ADC

PARAMETER	SPECIFICATION
Resolution	12-bit resolution (11-bit ENOB)
Sampling rate	650 megasamples per second
Input analog bandwidth	1.5 GHz
Digital output data format	LVDS
Analog supply voltage	2.5 V, 4.5 V
Digital supply voltage	1.2 V
Analog input voltage	1.0 V peak-to-peak (differential)
Input capacitance	5 pF
Input reference voltage	1.65 V (typ)
Power consumption	650 mW
Temperature range	-40 to +85 degrees C
Differential non-linearity (DNL)	<0.5 LSB
Integral non-linearity (INL)	<0.5 LSB
Area (excluding pads)	2.5 mm^2
Process	IBM 130 nm SiGe (8HP)

Ridgetop is AS9100C/ISO9001:2008 certified and has Trusted IC Design Supplier accreditation from U.S. Defense Microelectronics Activity (DMEA)

Need modified or custom design? Contact Ridgetop at 520-742-3300 to discuss your ideal solution!

Corporate Headquarters

3580 West Ina Road

Tucson, Arizona 85741 USA

OFFICE +1 520 742 3300

INFO@RIDGETOPGROUP.COM

Worldwide Locations

Support and sales locations for Ridgetop Group Inc. exist in Germany, Belgium, Japan, China, and the United States.

For office locations and contact information, please call the corporate headquarters or visit us on the web: **www.ridgetopgroup.com**