IC Process Characterization with ProChek™, a Compact Benchtop System

By

Esko Mikkola, Ph.D.

May 30, 2012
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- Brief History of ICs
- Trends in Reliability
- Degradation Mechanisms of Modern CMOS ICs
- ProChek Concepts
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  - Targeted Fabrication Processes and Test Results
- Summary
History of Integrated Circuits

First transistor, 1947

Size: 10 cm
Speed: Slow
Circuit Density: 0.0001 devices per 1 mm²
History of Integrated Circuits

Transistor, 2012

Size: 14 nm
Speed: >500 GHz
Circuit Density: 50,000,000 devices per 1 mm²

500,000,000,000X improvement in circuit density in 65 years!
History of Integrated Circuits

Size comparison, 35 nm MOSFET shown
History of Integrated Circuits

First “super computer,” 1947 (ENIAC, “the Giant Brain”)

Size: 1800 square feet
Performance: 5,000 FLOPS
Power: 150 kW
Reliability: >10 years

“Where a calculator on the ENIAC is equipped with 18,000 vacuum tubes and weighs 30 tons, computers of the future may have only 1,000 vacuum tubes and perhaps weigh 1½ tons.” – Popular Mechanics, March 1949.
History of Integrated Circuits

Microprocessor 2012

Size: 200 mm²
Performance: 1,000,000,000,000 FLOPS
Power: 100 W
Reliability: 10 years?

300,000,000,000X improvement in wattage/FLOP in 65 years!

How about reliability?
IC lifetime is becoming a serious concern

Failure rate

Infant mortality

Useful life

Wearout

[T. M. Mak]

Time

<7 year

~7 year

~10 year

90nm 130nm 180nm

~7 year

~10 year

[T. M. Mak]
Trends in IC Reliability

28 nm CMOS ring oscillator frequency degrades 5.5% within a year in normal operation conditions

Source: Synopsys
Time-zero parameter spread due to process mismatch shifts during the operational life due to degradation. Both process mismatch and degradation effects are worse in the smallest-geometry processes.

Source: “Low-Power Variation-Tolerant Design in Nanometer Silicon” By Swarup Bhunia
Cost of Reliability Problems

B-2 bomber crash in Guam Feb 2008.
   - $1.4B loss

Moisture in the transducers during calibration distorted the information in the air data system.

This caused the flight control computers to calculate inaccurate airspeed and negative angle of attack upon takeoff.

SANTA CLARA, Calif., Jan. 31, 2011 – As part of ongoing quality assurance, Intel Corporation has discovered a design issue in a recently released support chip, the Intel® 6 Series, code-named Cougar Point, and has implemented a silicon fix. In some cases, the Serial-ATA (SATA) ports within the chipsets may degrade over time, potentially impacting the performance or functionality of SATA-linked devices such as hard disk drives and DVD-drives. The chipset is utilized in PCs with Intel’s latest Second Generation Intel Core processors, code-named Sandy Bridge. … Intel expects this issue to reduce revenue by approximately $300 million as the company discontinues production of the current version of the chipset and begins manufacturing the new version. Full-year revenue is not expected to be materially affected by the issue. Total cost to repair and replace affected materials and systems in the market is estimated to be $700 million.

Source: Intel Newsroom
# Degradation Effects, Overview

<table>
<thead>
<tr>
<th>Failure Mode</th>
<th>Physics</th>
<th>System Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>NBTI (PMOS), PBTI (NMOS)</td>
<td>▪ Negative $V_T$ shift for PMOS, positive for NMOS</td>
<td>▪ Timing faults in processors other digital circuits</td>
</tr>
<tr>
<td></td>
<td>▪ Lower leakage and $I_{ON}$, slower speed</td>
<td>▪ Resettable – but increasing severity over time</td>
</tr>
<tr>
<td>TDDDB</td>
<td>▪ Soft breakdown:</td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ Slower speed</td>
<td>▪ Increased ESD vulnerability</td>
</tr>
<tr>
<td></td>
<td>▪ Weakened gate oxide</td>
<td>▪ Non-resettable timing faults</td>
</tr>
<tr>
<td></td>
<td>▪ Increased leakage current</td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ Hard breakdown</td>
<td>▪ Catastrophic short</td>
</tr>
<tr>
<td>Hot Carrier (NMOS)</td>
<td>▪ Positive $V_T$ shift</td>
<td>▪ Increased Off-state power</td>
</tr>
<tr>
<td></td>
<td>▪ Change in sub-threshold swing (transistor won’t turn OFF)</td>
<td>▪ Increased current draw</td>
</tr>
<tr>
<td></td>
<td>▪ Decreased data retention time in DRAM</td>
<td>▪ Decreased data retention time in DRAM</td>
</tr>
<tr>
<td>Metal Migration</td>
<td>▪ Higher resistance in Via connections</td>
<td>▪ Catastrophic open</td>
</tr>
<tr>
<td></td>
<td>▪ Open circuits</td>
<td></td>
</tr>
</tbody>
</table>
Via/metallization Failure Mechanisms: Electromigration and Stress Migration

45 nm Interconnects

- Loose pitch + thick metal on upper layers
  - High speed global wires
  - Low resistance power grid

- Tight pitch on lower layers
  - Maximum density for local interconnects

Modern CMOS processes have several metallization layers (up to a dozen).
Degradation Mechanisms: Electromigration

Electromigration Associated with Vias

(Pictorial)

(Actual)

Source: IRPS 2011 Tutorials
Electromigration (Temperature Dependency)

Reported data from fast Wafer Level Reliability (fWLR) tests shows that every 50°C increase in the stress temperature will reduce the electromigration testing time by one order of magnitude.

Stress Migration (Al Metallization)

Stress-Migration/Voiding-Rate in Al Metallization

McPherson & Dunn SM Model *

Aluminum
Creep-Rate Parameters:
\[ n=2.33, Q=0.58\text{eV}, \]
\[ T_c=232^\circ\text{C} \]

High Tensile Stress But Low Mobility

High Mobility But Low Tensile Stress

\[ C_{\text{Creep(Voiding)Rate}} = B_o (T_o - T)^n \exp \left( -\frac{Q}{K_B T} \right) \]


Conclusion: Peak occurs in the SM Rate for Al from 150-175\(^\circ\text{C}\).
Stress-Migration/Voiding-Rate in Cu

\[ \text{Creep.Voiding Rate} = B_o \left( T_o - T \right)^n \exp \left[ - \frac{Q}{K_B T} \right] \]

Conclusion: Peak occurs in the SM Rate for Cu from 175-200°C.

Source: IRPS 2011 Tutorials
Time-Dependent Dielectric Breakdown (TDBB)

Short caused by TDBB is seen in this thermal camera image.
TDDB (Types of Breakdown)

Thickenss-Dependent Features of TDDB

- **tox < 50Å**: Soft Breakdowns
- **Stress-Induced Leakage (tox < 100Å)**
- **tox > 100Å**

**Graph**:
- **I(t)**
- **t**
- **TDDB**

Source: IRPS 2011 Tutorials
TDDB (Types of Breakdown)

Criteria between TDDB types are not well-defined.

Source: IRPS 2011 Tutorials
TDDB (DC stress vs. AC stress)

DC and AC stresses may cause completely different results => Need to characterize both stress modes.

Source: IRPS 2011 Tutorials
Hot Carrier Degradation

Hot Carrier – Physics of Failure

Drain Avalanche Hot-Carrier Injection

- Impact ionization
  - Energetic electrons excite other e⁻’s from VB to CB
  - Holes created at VB
- Holes are attracted toward:
  - Substrate contact
  - Gate oxide (low $V_{GS}$)
- Electrons go toward:
  - Drain contact
  - Gate oxide (mid and high $V_{GS}$)
Hot Carrier Degradation

Hot-carrier induced effects

1. Parallel shift of I-V curve due to oxide trapped charge $N_{ot} \Rightarrow$ Increase in $V_T$
2. Stretch-out of I-V curve due to interface states $N_{it} \Rightarrow$ Decrease in ‘s’
3. Decrease in transconductance due to mobility degradation $\Rightarrow$ Decrease in $I_{D_{sat}}$
Hot Carrier Degradation

HCl Impact on NMOS Device Parameter

TF Depends on Critical Device Parameter

Gm
Idlin
Id, reversed
Id, forward

10 yr DC
1.0 yr DC
0.1 yr DC

TF [sec]
1E+10
1E+9
1E+8
1E+7
1E+6
1E+5
1E+4
1E+3

Isub [μA/μm]
0.1
1
10
100

Note: Time-To-Failure should be based on the critical device-parameter of interest

Source: IRPS 2011 Tutorials
## Hot Carrier Degradation

Fabs do not give enough reliability test data to designers and reliability engineers.

### Table: Hot Carrier Degradation Test Results

<table>
<thead>
<tr>
<th>Qual Items</th>
<th>DUT</th>
<th>Structures</th>
<th>Sample size</th>
<th>Stress Conditions</th>
<th>Failure Criteria</th>
<th>Specifications</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate oxide VBD</td>
<td>1.2V Core</td>
<td>Area = 562 × 2.483 μm²</td>
<td>&gt;1 wafer/lot; 3 lots; 25,560</td>
<td>Voltage ramp 3.3V/s (reversal mode)</td>
<td>I&lt;sub&gt;g&lt;/sub&gt; leak &gt; 40A @ 1V</td>
<td>Do = 5cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 12V</td>
<td>Do = 10cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 2.5V</td>
</tr>
<tr>
<td>Gate oxide VBD</td>
<td>2.5V I/O</td>
<td>Area = 4.6e3 × 1 μm²</td>
<td></td>
<td>Voltage ramp 6.27V/s (reversal mode)</td>
<td>I&lt;sub&gt;g&lt;/sub&gt; leak &gt; 16A @ 1.6V</td>
<td>Do = 5cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 2.4V</td>
<td>Do = 10cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 5.6V</td>
</tr>
<tr>
<td>Gate oxide VBD</td>
<td>2.5V I/O over drive</td>
<td>Area = 16e3 × 2 (WL=4.9 x 2000)</td>
<td>&gt;100 wafer/lot; 3 lots</td>
<td>Voltage ramp 6.27V/s (reversal mode)</td>
<td>I&lt;sub&gt;g&lt;/sub&gt; leak &gt; 10A @ 1.6V</td>
<td>Do = 5cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 3.3V</td>
<td>Do = 10cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 7.2V</td>
</tr>
<tr>
<td>PID</td>
<td>1.2V Core</td>
<td>WL=0.1</td>
<td>&gt;4 wafer/lot; 3 lots</td>
<td>I&lt;sub&gt;g&lt;/sub&gt; taling</td>
<td>I&lt;sub&gt;g&lt;/sub&gt; taling &lt; 5%</td>
<td>Do = 3cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 1.5V</td>
<td>Do = 3cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 2V</td>
</tr>
<tr>
<td>PID</td>
<td>2.5V I/O</td>
<td>WL=2.63/0.38</td>
<td></td>
<td></td>
<td></td>
<td>Do = 10cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 1.6V</td>
<td>Do = 20cm&lt;sup&gt;2&lt;/sup&gt; @ VBE = 1.6V</td>
</tr>
<tr>
<td>HCI</td>
<td>1.2V Core</td>
<td>WL=10/0.66</td>
<td>24 patterns lot; 3 lots</td>
<td>1.2V (V&lt;sub&gt;BV&lt;/sub&gt;=1V, 1.5V, 1.9V)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HCI</td>
<td>2.5V I/O</td>
<td>WL=10/0.28</td>
<td>15 patterns lot; 3 lots</td>
<td>2.5V (V&lt;sub&gt;BV&lt;/sub&gt;=3.3V, 3.5V, 3.7V, 10% of V&lt;sub&gt;DD&lt;/sub&gt;)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HCI</td>
<td>2.5V I/O over drive</td>
<td>WL=10/0.5 (N), 10/0.4 (P)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NBTI</td>
<td>1.2V Core</td>
<td>WL=10/0.66</td>
<td>&gt;20 lots; 3 lots</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NBTI</td>
<td>2.5V I/O</td>
<td>WL=10/0.28</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NBTI</td>
<td>2.5V I/O over drive</td>
<td>WL=10/0.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EM</td>
<td>M1 + contact</td>
<td>W=0.060/0.9 (1800 A)</td>
<td>&gt;20 patterns lot; 3 lots</td>
<td>J&lt;sub&gt;sat&lt;/sub&gt;=1-5mA/μm&lt;sup&gt;2&lt;/sup&gt; @ 300°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EM</td>
<td>M1 + Vi</td>
<td>W=0.1/0.10 (2200 A)</td>
<td></td>
<td>J&lt;sub&gt;sat&lt;/sub&gt;=1-5mA/μm&lt;sup&gt;2&lt;/sup&gt; @ 300°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EM</td>
<td>M1 + Vi</td>
<td>W=0.2/0.20 (2000 A)</td>
<td></td>
<td>J&lt;sub&gt;sat&lt;/sub&gt;=1-5mA/μm&lt;sup&gt;2&lt;/sup&gt; @ 300°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EM</td>
<td>Al-Cu RDL</td>
<td>W=3/2 (14.5k A)</td>
<td></td>
<td>J&lt;sub&gt;sat&lt;/sub&gt;=1-5mA/μm&lt;sup&gt;2&lt;/sup&gt; @ 250°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SM</td>
<td>Via chain</td>
<td>metal-via overlap from min to 0.7</td>
<td>&gt;130 lots; 3 lots</td>
<td>500 hr bake @ 175°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IMD Low-K TIEDB</td>
<td>M1, V1, M2 combi</td>
<td>M1 &amp; M2 W5/Min/Mn V1 W5=0.3/0.13</td>
<td>&gt;30 patterns lot; 3 lots</td>
<td>2.5-4.0 MA/cm&lt;sup&gt;2&lt;/sup&gt; @ 125°C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DC lifetime for Hot Carrier $>0.2$ yr, AC lifetime $>10$ yr in a 65 nm CMOS process.

http://www.siliconbluetech.com/media/downloads/SBT_65LP_Process_Qual_v0.1.pdf
During normal P-MOS operation, interfacial Si-H bonds can become broken. Negative gate voltage serves to produce more holes at the Si surface. Hole absorption by the Si-H bond can serve to free the hydrogen which can then can diffuse away from the Si-O interface resulting in interface-state generation and a $V_{th}$ shift. Si-H bonds are more easily broken at higher temperatures.

Source: IRPS 2011 Tutorials
PBTI is an issue in the modern “High K + Metal Gate” technologies.
NBTI and PBTI (High-K Gate)

NBTI/PBTI-induced $V_T$ drifts vs. stressed time for 32 nm poly-gate and high-k metal-gate devices.

NBTI and PBTI (Relaxation)

Example of PBTI Relaxation => Fast measurement is required.
NBTI and PBTI (DC vs. AC stress)

Impact of Stress Mode on PBTI Relaxation

Source: IRPS 2011 MG HK Tutorial

K. Zhao et al., IRPS, pp. 50-54, 2009.
Our Customers’ Problems

Customer 1:
“Foundries do not give us enough reliability test data”

Customer 2:
“We can test only three DUTs in parallel and the test lasts a full month”
Overview of the Existing Problem

- Small-geometry fabrication processes are very complex
- Reliability concerns for demanding applications include:
  - Bias Temperature Instabilities
  - Dielectric Breakdown
  - Hot Carrier Effects
  - Electromigration
  - Stress Migration
  - Process Mismatch Effects
  - Lot-to-lot Variation
- For space and radiation-sensitive applications there are also:
  - Single-event radiation effects
  - Total dose radiation effects
- Current techniques are not:
  - Comprehensive enough
  - Accurate enough
  - Fast enough
Solution: ProChek (Process Checker)

- Test Coupon
- Host Controller
- Test Card
- Benchtop Tester
What is ProChek?

ProChek is an innovative low-cost technique to very rapidly characterize the intrinsic reliability of deep submicron nanotechnology CMOS processes (bulk CMOS, SOI and SiGe)
Characteristics of ProChek

- Targets bulk CMOS, SOI, SiGe reliability concerns
  - NBTI / PBTI, TDDB, HC, EM, SM, TID
- Test Coupon
  - As little as 1 * 1 mm chip area
  - MPW for lower cost
  - 32 – 1024 devices can be tested in parallel for maximum throughput
  - On-chip per transistor heaters to 325 °C, greatly reducing test time
  - Synthesizable (except for on-chip heaters) to speed deployment
- Benchtop Tester
  - Fully programmable test conditions cover DC and AC stress cases
  - Portable and compact
  - ATE not needed
- Host Controller
  - Easy-to-use software GUI
  - Rich suite of built-in reliability test templates
  - Data processing capabilities
Structure of ProChek

- Test Type
- Test Bias
- Test Duration
- Result Collection
- Result Processing

HOST CONTROLLER + GUI

BENCHTOP TESTER

USB 2.0

RAM

MCU

Programmable sources

Prog. sources and I/V meas. devices

VIA/Contact DUTs

Transistor DUTs

Address Logic

DUTs

DUTs

DUTs

DUTs

DUTs

16 X 64 DUTs

…or more

Packaged chip on Test Card

TEST COUPON

V_S (0 – 5V, 0 – 1 MHz)

V_M (0 – 5V, 100 pA)
The Test Coupon is a packaged chip that contains arrays of DUTs that are addressed from serial package pins and stressed and measured with the high-resolution Benchtop Tester.
Local poly-silicon heaters capable of 325 °C will reduce EM, SM and BTI test time and cost.

With robust on-chip circuitry and local heaters, ProChek provides as high acceleration factor for package level reliability testing (PLR) on parallel DUTs as currently done for single DUTs in fast Wafer Level Reliability Testing (fWLR).
Thermal Simulation Results

According to 3D thermal simulations, the localized DUT arrays heat up to 325 °C in 75 milliseconds and consume 16 mW of power per DUT during the test. The temperature drops rapidly on the chip, so the non-stressed structures will not undergo any damage.
Measurement templates include:

- QBD
- TIDDB
- HCI / Vτ Shift
- HCI / Fast Sweep
- HCI / Slow sweep
- PBTI / Vτ Shift
- PBTI / Fast Sweep
- PBTI / Slow Sweep
- NBTI / Vτ Shift
- NBTI / Fast Sweep
- NBTI / Slow Sweep
- TID
- Via (Electromigration, Stress Migration)
### ProChek GUI: BTI Test

#### BTI test:

<table>
<thead>
<tr>
<th>Example of basic on-the-fly (OTF) measurement:</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Drain current is monitored during a single stress and a single relaxation phase.</td>
</tr>
<tr>
<td>• During stress: ( V_g = 0, V_s = V_b = V_{stress}, V_d = V_{stress} - 50 \text{ mV} ). Measure ( I_d ) 10 times per decade (logarithmic sampling rate), starting from ( 10^{-3} \text{ s} ) stopping at ( 10^4 \text{ s} ).</td>
</tr>
<tr>
<td>• During relaxation: ( V_g \approx V_{stress} -</td>
</tr>
</tbody>
</table>

#### Example (from analytical calculations, not measured):

![Graph showing stress and recovery time](image)

**Graph:**
- **X-axis:** stress time (s)
- **Y-axis:** \( \Delta V_{th} (\text{mV}) \)

![Graph showing recovery time](image)

**Graph:**
- **X-axis:** recovery time (s)
- **Y-axis:** \( \Delta V_{th} (\text{mV}) \)
ProChek Benchtop Tester connected to a laptop

Circuit boards inside the ProChek Benchtop Tester
Benchtop Tester Architecture

- **Computer GUI**
  - Test type,
  - Result collection,
  - Result processing

- **USB 2.0**

- **SD Slot**

**Main Test Board**

- **FPGA**

**Scenario Processor**

**Test Coupon**

- **FVMC Supplies**
- **FVMC / FCMV Supplies**
- **FCMV Temp. Meter**

**Measurement Utility Plug-in**

- **VMEAS (G,B)**
- **VMEAS (D,S,VIA)**
- **DIODE (Force,Sense)**

**Stress Utility Plug-in**

- **TC Supply**
- **TC SR Control**
- **Heater / Cooler**
- **Stress Supplies**

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**Ridgetop Group Inc**

3580 West Ina Road | Tucson AZ | 85741 | 520-742-3300 | ridgetopgroup.com
ProChek Test Results: Hot Carrier

TSMC 65GP, Test Coupon #23, 100hr HCl test, room T, min. size NMOS

VT [V]

Stress Time [hrs]

Zoom-in, first five DUTs

VT [V]

Stress Time [hrs]
ProChek Test Results: V-ramp to Breakdown

TSMC65GP, TC #7, V-ramp to BD, room T, min. size NMOS

\[ V_S = V_D = V_B = 0.0V \]
ProChek Test Coupons: Targeted Processes

**IBM 12 SO**
- 45 nm SOI
- NMOS, PMOS
- 64 DUTs
- < 1 mm²
- June 2010

**TSMC 65 GP**
- 65 nm CMOS
- NMOS, PMOS, via
- 96 DUTs
- < 1 mm²
- April 2011

**IBM 9LP**
- 90 nm CMOS
- NMOS, PMOS, via, RO
- 203 DUTs (incl. 5 ROs)
- < 2 mm²
- October 2011

**IBM 9SF**
- 90 nm CMOS
- NMOS, PMOS, via, RO
- 203 DUTs (incl. 5 ROs)
- < 2 mm²
- March 2012

**IBM 10LPe**
- 65 nm CMOS
- NMOS, PMOS, via
- 1200 DUTs
- 4 mm²
- May 2011

**TowerJazz**
- 180 nm SiGe
- NMOS, PMOS, HBT, annular
- 96 DUTs
- < 1 mm²
- August 2011

**IBM 8HP**
- 130 nm SiGe
- NMOS, PMOS, HBT, RHBD RO
- 330 DUTs
- 4 mm²
- January 2012
Summary

- ProChek is an advanced new tool for fabrication process qualification that offers significant advantage to IC designers and reliability engineers
  - Cost and time budgets of fabrication process qualification are significantly reduced
  - Covers (all) the reliability concerns of modern nanotechnology processes
Questions?
## Upcoming Webinars

<table>
<thead>
<tr>
<th>Topic</th>
<th>Date</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Implementation of Prognostics in Solar Applications</td>
<td>Wed. Jun 27, 2012</td>
<td>1:00 - 2:00 PM PDT</td>
</tr>
<tr>
<td>Troubleshooting Analysis and Decision Support in Complex Applications</td>
<td>Wed. Jul 25, 2012</td>
<td>1:00 - 2:00 PM PDT</td>
</tr>
</tbody>
</table>

For more information about Ridgetop Group Webinars, email us at information@ridgetopgroup.com
Thank you!

Ridgetop Group, Inc.

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