A Sensor for Real-Time Detection of Solder-Joint Faults in Operational Field Programmable Gate Arrays

By James Hofmeister, Justin Judkins, Douglas Goodman, Edgar Ortiz
Ridgetop Group, Inc.
3580 West Ina Road, Tucson, AZ, 85741, USA

1. INTRODUCTION

The authors present a sensor for real-time detection of solder-joint faults in programmed, operational Field Programmable Gate Arrays (FPGAs), especially those FPGAs in Ball Grid Array (BGA) packages, such as a XILINX® FG1156 [1]. FPGAs are used in all manner and kinds of control systems in aerospace applications. The ability to sense high-resistance faults in the solder joints of operational FPGAs increases both fault coverage and electronic Prognostics Health Management (ePHM) capabilities and support for condition-based and reliability-centered maintenance. As both the pitch between the solder balls of the solder joints of BGA packages and the diameter of the solder balls decrease, the importance of this sensor increases.

The Sentinel SJ BIST™ sensor presented in this paper detects high-resistance faults, including opens, in operational I/O networks of programmed, operational FPGAs. It is realized as a two-pin test group core that was designed, programmed in a hardware description language, simulated, synthesized and loaded into an FPGA. SJ BIST correctly detects and reports instances of high-resistance with zero false alarms: test results are shown in this paper. The test program, which contains temporary data collection routines for statistical analysis, uses less than 250 cells out of over 78,000 cells for a 5-million gate, 1156-pin FPGA to test 8 corner pins. Initial testing indicates SJ BIST is capable of detecting high-resistance faults as least as high as 100 Ω, which last one-half a clock period or longer.

In addition to producing no false alarms in the current period of testing, SJ BIST will not introduce additional failure mechanisms to an assembly. This is SJ BIST, with the exception of small capacitors, (1) is not invasive to an application program; (2) is not compute intensive and so timing problems are not anticipated; and (3) failures in SJ BIST are either going to result in no alarms or they will report alarms, which correctly indicate reduced reliability in the assembly.

Mechanics of Failure

Solder-joint fatigue damage is cumulative and is typically caused by thermo-mechanical and shock stresses. Fatigue damage manifests as voids and cracks, which propagate in number and size. Eventually, the solder joint fractures [2-5] and FGPA operational failures occur. An illustration of a damaged solder joint (or bump) on the verge of fracturing is shown in Figure 1.

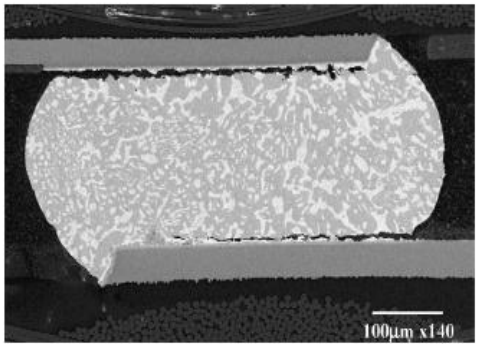

Figure 1: Crack Propagation at the Top and Bottom of a Solder Joint, 15mm BGA [3].

A significant cause of solder-joint fatigue damage is thermo-mechanical stress, especially in the horizontal direction as shown in Figure 2 because of the following [5-7]:

(1) Differences in coefficients of thermal expansion of the materials in the FPGA, the solder, the wiring, the interconnections and the printed wire board (PWB).

(2) Heating and cooling due to ambient temperature changes and to power-on and -off cycling. For example, grain boundaries in solder material continues to grow even when power is removed; increased grain boundaries lead to increased voids, which lead to increased onset of cracks.

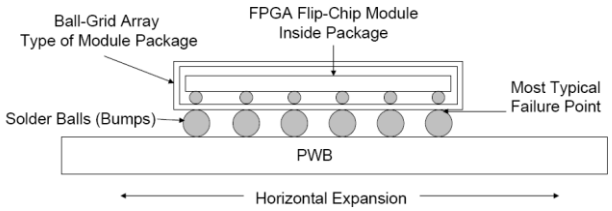

Figure 2: FPGA Package, Solder Ball and Printed Wire Board Diagram Showing a Typical Failure Point.

Fatigue damage can also accumulate because of stresses from shock, vibration and torque forces to which the

assembled PWB is subjected to during missions, maintenance and storage. The accumulative damage eventually causes the solder joint to fracture, typically at the boundary of the solder ball and the package or at the boundary of the solder ball and the PWB, as seen in Figure 1 and Figure 2.

There are many possible points of failure in a solder-joint network. Referring to Figure 3, typical failure types and points are the following:

(1) Open in the wiring of the die between the buffers of an I/O port and the small solder bump.

(2) Open in the wire connection between the package and the die.

(3) Crack in the connection between the FPGA die and the outside of the chip module package.

(4) Crack through the solder bump.

(5) Crack between a solder bump and the wiring on a PWB.

SJ BIST is not sensitive or dependent upon a particular failure type or point of failure location.

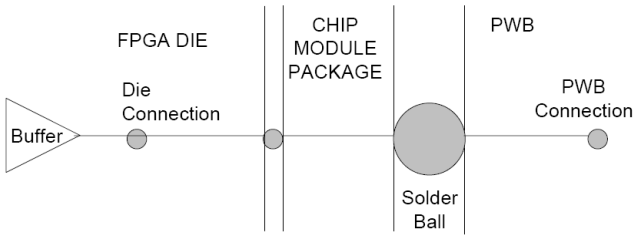

Figure 3: Simplified Representation of a Solder-Joint Network.

Subsequent mechanical vibration or shock tends to cause such fractured bumps to momentarily open and cause hard-to-diagnose faults of high resistance of hundreds of ohms or higher and lasting for periods of hundreds of nanoseconds, or less, to more than 1 μs [2, 5, 6, 8-11]. These intermittent faults in solder-joint networks increase in frequency as evidenced by a practice of logging BGA package failures only after multiple events of high-resistance: an initial event followed by some number (for example, 2 to 10) of additional events within a specified period of time, such as ten percent of the number of cycles of the initial event [9-11]. Even then, an intermittent fault of high-resistance in a solder-joint network might not result in an operational fault. For example, the high-resistance fault might happen in a single ground or power connection (where there are many other ground and power connections for the FPGA circuitry), or it might happen during a period when the network is not being written, or it might be too short in duration to cause a signal error. Figure 4 shows shock-actuated intermittent opens (high resistance).

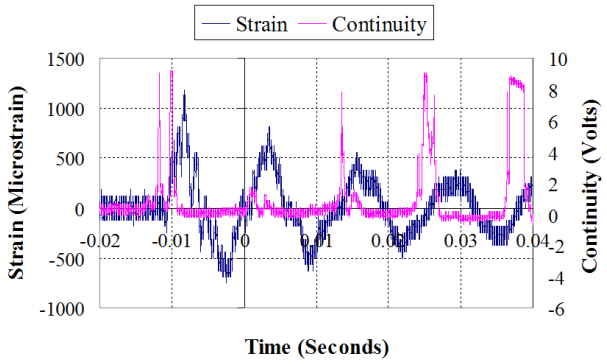

Figure 4: Shock-Actuated Failure - Transient Strain and Resistance (from Lall).

Location of Greatest Stress on FPGA I/O Ports

The I/O pins, which are the solder balls, of an FPGA nearest the edges of the BGA package, especially those nearest to one of the four corners of a BGA package or die, experience the greatest thermo-mechanical stresses [12-15]. This is a good reason why the four solder joint locations at the corners of a XILINX FG1156 are connected to ground. This means that I/O pins on the outer edge of the BGA package that are near to one of the four corners are strong candidates for selection as SJ BIST test pins – those pins are likely to fail first.

State of the Art

In previous work, the authors have demonstrated the use of precursor indicators of failure for prognostication of electronics [12-15]. One important reason for using SJ BIST is stress magnitudes are hard to derive, much less keep track of, which leads to inaccurate life expectancy predictions [16]. Another reason for using SJ BIST is that even though a particular damaged solder-joint network (I/O port and the I/O pin circuit) might not result in immediate FPGA operational failure, the damage indicates the FPGA is likely to have other I/O pins that are damaged, which means the FPGA is no longer reliable. SJ BIST could also be used in newly designed manufacturing reliability tests to address a concern that failure modes caused by the PWB-FPGA assembly are not being detected during component qualification [7].

Modern FPGAs with millions of transistors are packaged as fine-pitch BGAs and ultra-pitch BGAs, such as the fine-pitch XILINX FG1156, and the packages have more than a thousand I/O pins and very small pitch and ball sizes. The XILINX FG1156, packaged as fine-pitch BGA has a 34 x 34 array of nominal 0.60 mm solder balls with a pitch of 1.0 mm (see Figure 5). This tends to make physical inspection techniques impractical and not useful.

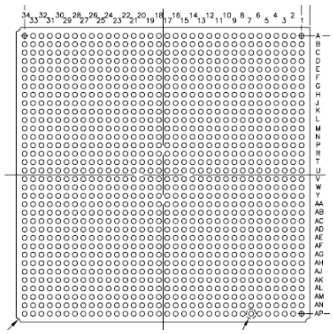

Figure 5: Bottom View of a XILINX FG1156 – Package Size is 35 x 35 mm with a 34 x 34 Array of Solder Balls of Nominal Diameter of 0.6 mm and a Pitch of 1.0mm[1].

Prior to SJ BIST, there were no known methods for detecting faults in operational, fully-programmed FPGAs. Furthermore, FPGAs are not amenable to the measurement techniques typically used in manufacturing reliability tests such as Highly Accelerated Life Tests (HALTs) [5]. This is because those measurement techniques require devices to be powered-off, and because FPGA I/O pins are connected to complex I/O port circuits, a representative I/O port circuit is shown in Figure 6. As seen in the figure, I/O ports contain tri-state buffers, diodes, resistors and logic input gates, which makes it difficult to detect damage to a solder-joint network, such as a high increase in resistance of the solder ball that attaches the FPGA I/O circuitry to the board.

2. REAL-TIME SOLDER JOINT SENSOR

The innovative, in-situ SJ BIST method requires the attachment of a small capacitor to a test group of two non-flight functional I/O pins that are connected together. Preferably two unused I/O pins nearest a corner of the FPGA package are selected for testing as a two-pin group, and for good results, there should be one two-pin group for each corner. Figure 6 shows the I/O port circuitry for a single I/O pin for a XILINX FG1156.

Figure 7 shows the block diagram of the SJ core (PC), inside of a FPGA on an application board. SJ BIST writes logical '1s' and '0s' to charge and discharge the capacitor and performs read checks. The occurrence of a high-resistance fault causes the capacitor to not fully charge, and a logical '0' instead of logical '1' is read by SJ BIST. A fault is detected and fault counts and signals are recorded for prognostic use.

SJ BIST Test – Figure 8 shows a test result: FPGA 10 MHz clock with no fault and with 100 Ω–fault injection on one of the I/O pins of a two-port test group. Various tests at 100 kHz, 1 MHz, 10 MHz, 20 MHz and 48 MHz were entirely successful: all instances of 100 Ω or higher faults were detected and reported with zero false alarms.

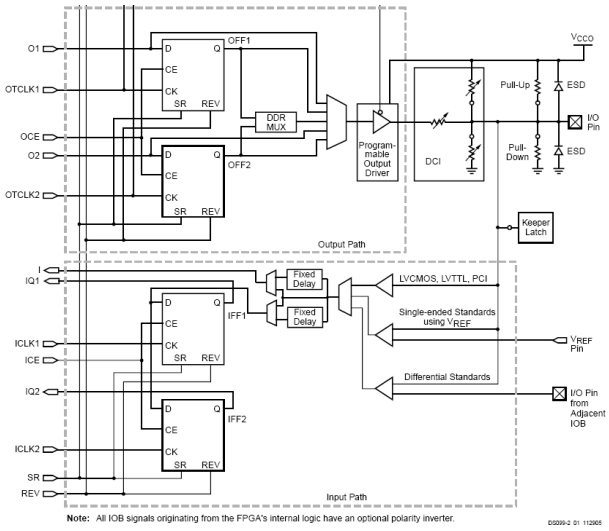

Figure 6: Diagram Showing Input and Output Buffers - FG1156, XILINX Spartan Series [1].

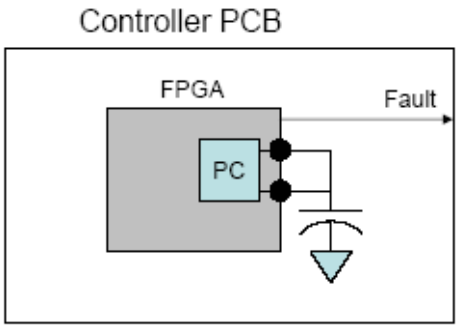

Figure 7: Block Diagram, SJ BIST in Application FPGA.

SJ BIST Plots – Figure 9 is a family of curves that show the relationship of FPGA clock frequency, detectable resistance and external capacitor value.

As expected, as the clock frequency is increased, the value of the external capacitor needs to be reduced. The left-most plot in Figure 9 exhibits interaction between the parasitic (intrinsic) capacitance of the I/O port and the impedance, both resistive and capacitive, of the oscilloscope. With a clock frequency of 48 MHz, SJ BIST produced correct results simply by connecting the two I/O pins together – SJ BIST also produced correct results at that frequency with a very small, externally-attached capacitor.

3. SJ BIST SIGNALS

Signals and Controls

SJ BIST, at minimum, must present at least one error signal (a fault indicator) either to an external FPGA I/O port or to an internal fault management program. For evaluation and

investigation, the prototype SJ BIST core provides two fault signals plus fault counts.

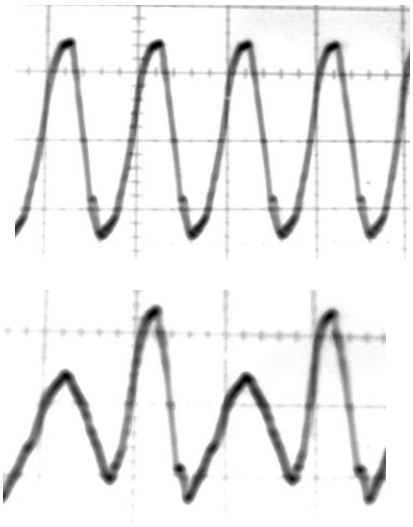

Figure 8: SJ BIST Test, Two-Port Group; No-Fault Result on the Top, 100Ω-Fault Result on the Bottom; 10 MHz Clock, 1V-100nS Grid.

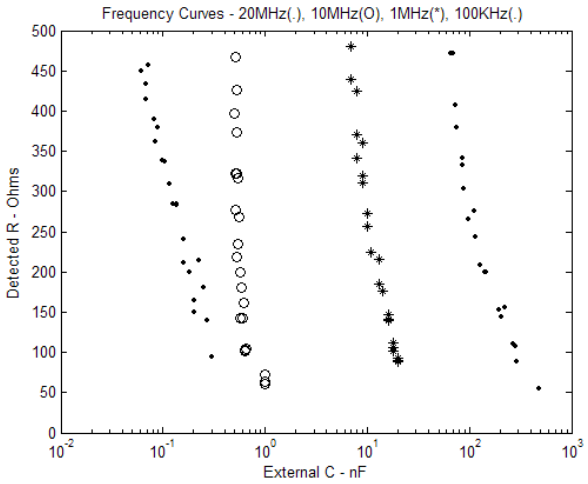

Figure 9: Family of Curves Showing the R, C and the Clock Frequency Relationship.

SJ BIST accepts control signals to enable, to disable and to reset the test, the signals and the counts.

Error Signal and Count – There are two fault signals as follows for each tested I/O pin: (1) at least one fault has been detected, and (2) a fault is currently active. For a multiple-pin test, these signals can be ORed together. SJ BIST also produces a count of the number of detected faults for each tested I/O pin: 8-bit, 255-count.

For a deployed SJ BIST, we anticipate most applications would only use the two error signals. We also believe a deployed SJ BIST application would most likely use at least four cores of 2-pin groups – one core for each corner of an FPGA.

Controls – In addition to CLK, SJ BIST has two input-control signals: ENABLE and RESET. ENABLE is used to turn SJ BIST detection on and off; RESET is used to reset both the fault signal latches and the fault counters. For a deployed SJ BIST, RESET might not be used.

SJ BIST Considerations

For "guaranteed" detection of a fault, a two-port, two-pin-test SJ BIST requires two clock cycles to test both pins. SJ BIST is capable of detecting faults that last for less than one-half of clock period, but only if the fault occurs at the beginning of write for that I/O pin.

To test 8 I/O pins, SJ BIST requires 4 external capacitors and 200 mW of power at 3.3 V.

4. CONCLUSION AND SUMMARY

In this paper we presented an overview of the physics of failure associated with the solder joints of FPGAs in BGA packages: the primary contributor to fatigue damage is thermo-mechanical stresses related to CTE mismatches, shock and vibration, and power on-off sequencing. Solder-joint fatigue damage can result in fractures that cause intermittent instances of high-resistance spikes that are hard-to-diagnose. In reliability testing, OPENs (faults) are often characterized by spikes of a couple of hundred ohms or higher that last for 200ns to 1μs or longer.

SJ BIST uses a method with programmed cores in-situ within the FPGA plus a small capacitor attached to each two-pin test group. Initial testing indicates SJ BIST is capable of detecting high-resistance faults at least as high as 100 Ω and which last one-half a clock period or longer.

Prior to SJ BIST, there were no known methods for detecting high-resistance faults in solder-joint networks belonging to operational, fully-programmed FPGAs.

SJ BIST is an important addition to prognostic health and management because stress magnitudes are hard to derive, which leads to inaccurate life expectancy predictions; and even though a particular damaged solder-joint port might not result in immediate FPGA operational failure, the damage indicates the FPGA is no longer reliable. An in-situ SJ BIST can also be used in newly designed manufacturing reliability tests to investigate failure modes related to the PWB-FPGA assembly. Absent SJ BIST, there is a serious lack of capability given the current direction and progress in

designing and implementing an electronic prognostic schema..

The two-port SJ BIST was programmed, simulated, synthesized, loaded into a FPGA on a development board and tested in a laboratory. The test results show the SJ BIST core correctly detects and reports instances of high-resistance without false errors – no errors detected or reported when the network resistance is 1.0 Ω or less.

INTELLECTUAL PROPERTY

A preliminary patent disclosure and a final patent have been filed: P.S. Spuhler, V.M. Vermeire and J.P. Hofmeister, "Method and circuit for the detection of solder-joint failures in a digital electronic package," final patent filing, published US-2006-0194353-A1, Aug. 31. 2006.

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