STATISTICAL PATTERN RECOGNITION AND BUILT-IN RELIABILITY TEST FOR FEATURE EXTRACTION AND HEALTH MONITORING OF ELECTRONICS UNDER SHOCK LOADS

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ABSTRACT

Failures in electronic equipment may are detected by diagnosing loss of functionality or loss of continuity. The proposed research focuses on the pre-failure space and presents methodologies for quantification of failure in electronic equipment subjected to shock and vibration loads using the dynamic response of the electronic equipment. The presented methodologies are applicable at the system-level for identification of impending failures and trigger repair or replacement significantly prior to failure.

Presently, the built-in stress test (BIST) is extensively used for diagnostics or identification of failure. The BIST approach has been applied to the testing of Digital chips and systems [Hashempour et.al. 2004], Internal and External Memories like DDR, QDR, Double DDR SRAM, FCRAM, and RLDRAM [Kim et.al 2004], ASICs [Sato et.al. 2001], and Mixed-Signal BIST applied on devices like ADCs, DACs, filters, amplifiers, power regulators, mixers [Sunter 2002, Huang et.al. 2000]. Built-In self tests have also been applied to the functional testing of FPGAs, testing the core logic block, the memory and various interconnect faults [Dutt 2006, Abramovici et.al. 2004, Liu et.al. 2003, Sun et.al. 2000, Stroud et.al. 1998]. The BIST approach has also been applied to testing of MEMS Accelerometers [Deb et.al. 2006] and Industrial circuits [Kiefer et.al. 2000] but the current version of BIST approach is focused on reactive failure detection and provides limited insight in to reliability and residual life.

The proposed approach can be extended to monitor product-level damage both during vertical and horizontal drops. Three methodologies have been investigated for feature extraction and health monitoring including development of a new solder-interconnect built-in reliability test, FFT based statistical-pattern recognition, and time-frequency moments based statistical pattern recognition.

The first approach includes a solder-joint built-in-reliability-test (SJ-BIRT) for detecting high-resistance and intermittent faults in operational, fully programmed field programmable gate arrays (FPGAs). The approach is simple to implement, offers a method to detect high-resistance faults that result from damaged solder joints, and uses a maximum of one small capacitor externally connected to each selected test pin or each group of two test pins.

In addition, statistical pattern recognition and leading indicators of shock-damage have been used to study the damage initiation and progression in shock and drop of electronic assemblies. Statistical pattern recognition is currently being employed in a variety of engineering and scientific disciplines such as biology, psychology, medicine, marketing, artificial intelligence, computer vision and remote sensing [Jain, et. al. 2000]. Previously, SPR based on wavelet packet energy decomposition and the Mahalanobis distance approach were studied for quantification of shock damage in electronic assemblies [Lall, et. al. 2006].

In this paper, the use of FFT based statistical-pattern recognition, and time-frequency moments based statistical pattern recognition has been investigated. Closed-form models have been developed for the eigen-frequencies and mode-shapes of electronic assemblies with various boundary conditions and component placement configurations. Model predictions have been validated with experimental data from modal analysis. Pristine configurations have been perturbed to quantify the degradation in confidence values with progression of damage. Sensitivity of leading indicators of shock-damage to subtle changes in boundary conditions, effective flexural rigidity, and transient strain response have been quantified.

Explicit finite element models have been developed and various kinds of failure modes have been simulated such as solder ball cracking, package falloff and solder ball failure. Models using cohesive elements [Towashiraporn, et. al. 2006] present at the solder joint-copper pad interface at both the PCB and package side have also been created to study the traction-separation behavior of solder. Cohesive zone modeling enables the detection of dynamic crack initiation and propagation leading to IMC brittle failure in PCB assemblies subject to drop impact.

The above damage monitoring approach is not based on electrical continuity and hence can be applied to any electronic assembly structure irrespective of the interconnections. The damage index developed provides parametric damage progression data, thus removing the limitation of current failure testing, where the damage progression can not be monitored. Hence the proposed method does not require the assumption that the failure occurs abruptly after some number of drops and can be extended to product level drops.