Reliability Challenges in Through-Silicon Via (TSV)-Based Packaging

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Agenda

- Problem Statement
- Interconnect Reliability – Background
- TSV BIST Detection Approaches
  - SJ BIST Overview
  - Precision Current Monitoring Overview
- Summary
TSV-based 2.5D & 3D ICs

- Stacking ICs with Through-Silicon Vias (TSVs)
  - Circuit density
  - Heterogeneous process integration
  - Speed/power
- Alternative to Pure “Moore’s Law” Improvements
- 3D ICs use TSVs to stack directly on each other
- 2.5D ICs stack with an interposer to route signals
- Test methods are both new and extensions to existing
Existing Approaches to 2.5D/3D IC Test

- “Known Good Die” → “Pretty Good Die”
- Finding Defects Prior to Shipment
  - X-ray, Optical Inspection
  - Boundary Scan (IEEE 1149.1)
  - IEEE P1838, others
- Limited Focus
  - Opens & shorts
  - Primarily digital
  - Static / low speed operation
  - Thermal issues?... Assembly complexities?...
- ...Reliability = Performance Over Time
Reported electronic system problems in the field cannot be duplicated at the service point or in the lab

“Three/Four-letter” words (CND, NTF, RTOK)
- Could Not Duplicate (CND)
- No Trouble Found (NTF)
- Retest OK (RTOK)

50 to 80% of these CND/NTF/RTOK problem categories are reported by service personnel.

Major culprits – Solder joint intermittencies and NBTI effects in deep submicron ICs
BGA Example: Cracks and Fractures

IC / SOC / SiP

Printed Circuit Board

Solder Balls

Typical Failure Points

Fractures

Lall 2005 IEEE
Defects: Location of Cracks/Fractures

- Corner pins likely to fail first
  - High stress areas, and corners of the package and die
Fatigue fractures (cracks) are caused by thermo-mechanical stress/strain.

During periods of high stress, fractured bumps tend to momentarily open and cause intermittent faults of high resistance for periods of ns to µs.

Over time, contamination and oxidation films occur on the fractured faces: the effective contact area becomes smaller and smaller.

Transient opens can be detected by event detectors.
Mechanics of Failure

HALT results - Pulled FPGA – Damaged Solder Balls

Undamaged

Damaged: Cracked

Cracked, not detectable

Fractured, detectable
Increased Complexity: 2.5D IC Interposer

**Si-BT Flip Chip Interposer**

*Flip Chip TSV Silicon Interposer*

- TSV
- Interconnect layers on one side or both sides
  - Cu/Pt interconnect layers on one surface (5 μm lines/spaces)
  - CMOS backend layers (1μm lines and spaces) with Backside TSV
- Built in Capacitor (1500 nF/cm² +)
- Solder Bump or Cu Pillar on the backside
- Smallest (Chip Size) Interposer for Cost and Reliability

Fine pitch flip chip solder bumps (<150μm)

**Diagram:**
- Cu Spreader / Heat Sink Attach
- Capacitors
- TSVs
- Simple BT or Ceramic substrate
- Flip Chip TSV based Si interposer with routing layers and decoupling capacitors (1500nF/cm² +)
- Under filled flip chip attach
2.5D interconnection challenges

- Undesired side effects of 2.5D ICs
  - Increased density $\Rightarrow$ increased heat $\Rightarrow$ degradation and defects
  - Qualification/testing is very difficult and expensive

- Confidence in 2.5D IC interconnect reliability must be raised

- Techniques for anticipating failure do not currently exist
  - Boundary scan standards for assembly testing are emerging but...
  - Boundary scan doesn’t address active in situ reliability issues

- Net effect on adopting 2.5D IC technology:
  - High level of preventive maintenance whenever possible
  - Avoidance when such maintenance is not possible, practical, or economical
Ridgetop 2.5D/3D IC Reliability System

- Proven BIST methodologies
- Real-time monitoring of interconnection integrity
  - Monitors degradation
  - Warns of impending failure (prognostic “canary cell”)
  - Detects and identifies intermittencies
- Covers both analog and digital signals
- Two alternate approaches (discussed in detail later)
Through-Silicon Via Built-In Self-Test (TSV BIST) Detection Approaches

SJ BIST
Q-Star Test PG-Mon

And, by the way...
TSV BIST monitors apply to other stacked die or multi-chip packaging approaches as well
Intermittent Faults in Components

- Faults are intermittent: confirmed by CAVE, Auburn Univ., German automobile manufacturer
  - Occur during periods of increasing strain
  - Multiple occurrences per cycle
  - Industry standard: 200 ohms +, 200 ns +
What is SJ BIST?

- SJ BIST = Solder Joint Built-in Self-Test
  - Original solution enabling the verification and validation of solder joint interconnect reliability
  - Originally developed for FPGA-BGA applications
  - Can be applied to validate the integrity and reliability of any type of interconnection
  - Can be instantiated via Verilog or VHDL for FPGAs
  - Software Executable version for CPUs
SJ BIST Implementation – Fault Sensor

- Verilog firmware core
  - Each core tests two I/O pins
  - Pins are externally wired together
  - Small capacitor connected to the two pins
SJ BIST Results

- LVTTL – Low Voltage TTL

**Input**
- Low ≤0.8V
- High ≥2.0V

**Output**
- Low ≤0.4V
- High ≥2.4V
SJ BIST Background

- Heritage
  - In situ interconnect reliability testing of high pin-count FPGAs in BGA packages
  - Originally developed for DoD & NASA space applications
- Proven and reliable
  - Easy to deploy
  - Highly sensitive to intermittencies and faults
    → Tunable for different operating frequencies
  - No “false positive” flags
- Extended to high density digital interconnection environment, i.e., 2.5D/3D ICs
SJ BIST Application

Requirement:
Interconnect path dedicated for SJ BIST

On-chip interconnects

Die to substrate (incl. bumps)

Die to board (incl. bumps & balls)
SJ BIST Application

Testing Die to Substrate

- SJ BIST logic core
- On-chip interconnect metal, vias, contacts
- Bump
- Substrate interconnect
- Substrate

= Interconnect path being tested
Testing On-chip Interconnect

Need for dedicated on-chip path between SJ BIST observation pins
SJ BIST Application

Testing Die to Board

SJ BIST logic core
On-chip interconnect metal, vias, contacts
Bump
Substrate interconnect
Substrate
Ball
Socket or board interconnect

= Interconnect path being tested
SJ BIST Application Results

- Independent test results by German automotive firm
  - Confirmed the same results as obtained by Ridgetop Group
  - No false alarms

![Graph showing 300 Ohm Fault](image-url)
Q-Star Test PG-Mon

Precision Current Measurement Approach
Precision Current Measurements

- **Q-Star Test current monitors**
  - **Modules**
    - Packaged part testing, lab characterization, failure analysis
    - $I_{\text{DDQ}}, I_{\text{DDT}}, I_{\text{SSQ}}$, power profiling, etc.
  - **On-chip monitors**
    - PG-Mon: validates power, ground, and other connections
    - T-Mon: monitors transient currents
Precision Current Measurement: Q-Star Test

- \( I_{\text{DDQ}}, I_{\text{DDT}}, I_{\text{SSQ}} \) and other precision picoamp level current measurement instruments for characterization and test
- On-board modules and on-chip sensors
- Test and DFT consulting and training services
- 70 semiconductor companies and 800 instruments installed
- Developed by Ridgetop Europe
PG-Mon Application 1

- On-chip I/O and power/ground connection verification
- Highly sensitive (1.5 - 4Ω), non-intrusive observation of signals

Example: IC Power Distribution Network Reliability Monitoring

Example: VDD Monitor Block Schematic
2.5D IC Reliability: Test Infrastructure Die

- “Test Infrastructure” die: Connects to strategic traces routed through the interposer
  - Most critical functionality
  - Most sensitive to degradation (e.g., corners or centers of Die 2 or Die 3)
  - Can monitor many signals
- SJ BIST/Q-STAR IP embedded in Test Infrastructure die
- Advantages
  - Minimizes interposer overhead
  - Low cost IC
  - Upgrades are simple
- Disadvantages
  - Extra interposer real estate
  - Distance from some signals

2.5D IC Reliability: SJ BIST & Q-Star monitors embedded in a Test Infrastructure Die
2.5D IC Reliability: Interposer-hosted

- Directly hosted on Interposer: Connects to strategic traces routed through the interposer
  - Most critical functionality
  - Most sensitive to degradation (e.g., corners or centers of Die 2 or Die 3)
  - Can monitor many signals
- SJ BIST/Q-Star IP embedded in Silicon Interposer
- Advantages
  - Minimizes interposer overhead
  - Monitors near key signals
- Disadvantages
  - Interposer cost is higher
  - Signal routing may be trickier

2.5D IC Reliability: SJ BIST & Q-Star monitors embedded in Silicon Interposer
From 2.5D IC to 3D IC Reliability Monitoring

- 3D IC migration: Embed SJ BIST / PG-Mon IP in TSV-enabled ICs
- Required when no interposer present
- Highest quality monitoring
- Reduces cost and overhead
- Standardized approach for broadest applicability
Summary

- 2.5D / 3D IC technologies pose new challenges
- Reliability assurance requires more than traditional test
- Real-time TSV BIST monitors...
  - Detect intermittencies
  - Identify degradation before failure
  - Are non-intrusive
Incorporated in 2000, and headquartered in Tucson, AZ. Ridgetop Europe established in 2010 in Belgium.

Microelectronic Design and Test Solutions:
- SJ BIST™ Based Test Solutions
- ProChek™ Semiconductor Characterization System
- Q-Star Test™ Precision Current Measurement Instruments
- PDKChek™ In-Situ Test Structures
- ISO:9001/AS9100C-compliant Design and Integration Services

Strong market position with commercial and government customers in USA, Canada, Europe, and Asia
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- E-mail follow-up questions & comments to
  - Tezzaron: David Chapman, dchapman@tezzaron.com
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Thanks for your time and interest!