Intermittent Fault Detection in Circuit Boards and Connectors

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October 8, 2014
Agenda

- Interconnect Reliability – Background
- SJ BIST Basics
- SJ BIST Operation
- SJ BIST Application
- Summary & Conclusions
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Interconnects are subject to

- Manufacturing defects
- Aging effects (electromigration)
- Stress (thermal, electrical, chemical, mechanical, vibration)
Causes of Interconnect Failure

- Bad soldering process
- Bad PCB manufacturing process
- Weak cable
- Bad connectors
- Thermal Stress
  - Differences in Thermal Expansion Coefficients (TCE) of different materials cause differences in expansion/compression
    → Heating / Cooling cycles
      • Changes in work load
      • Changes in ambient
      • Power-on / Power-off cycling
- Mechanical Stress
  - Shock – Vibration – Torque – Bending
  - Mission – Maintenance – Storage conditions
Solder Joint Failure

- Solder joints are susceptible to mechanical failure leading to opens, shorts or intermittencies and affecting functional and electrical signal behavior
  - Primary Causes of Solder Joint Failure:
    - Bad solder process
    - Low quality solder material
    - Thermal stresses
    - Physical Stress
    - Missing Solder Ball
  - Leading to
    - Increased Resistance
    - Intermittent Signal
    - Cracks and Fractures
An interconnect intermittent fault is an event that causes the interconnect resistance to increase for a predefined amount and last for a minimum time.

Fault detection is linked to # of occurrences

Definition evolved:
- From: R increase of $1\text{K}\Omega$ lasting at least 1$\mu$s
  → JEDEC 22-B111
- To: R increase of 200$\Omega$ lasting at least 200ns

Interconnect is classified as failing if subsequent to the occurrence of the first event, nine more events are detected that occur within a period of time $T_2$ that is less than or equal to 10% of the time to the occurrence of the first event $T_1$. ($T_2 \leq 0.1*T_1$)
In manufacturing reliability and lifetime Qualification tests, a single instance of a high-resistance spike (a fault) is not considered a package failure.

A package failure is typically defined as either:
- High frequency of events
- High count of events

An event (a fault) is typically defined by the industry as a detected high-resistance spike of 200 to 300 ohms or more that lasts for 200 nanoseconds or longer.
Reliability Manufacturing and Package Failure Criteria

- High Frequency of Events Failure
  - In a typical lifetime test, the number of cycles (time) between the start of the test and the first detected high-resistance spike is recorded as time T1. A package is deemed to have failed when an additional nine events are detected in a period of time (T2) that is less than or equal to 10% of the T1 time period.
  
  → This method of evaluation requires a minimum of 10 events for a package to be recorded as having failed.

- Multiple Count of Events Failure
  - In a typical lifetime test, an open is defined as two or more events that occur in the same cycle. A package is deemed to have failed when 15 opens occur.
BGA – PCB Relationship: Die, package, wiring, pins

34x34 array of balls
1 mm pitch

Common fracture locations
Defects: Location of Cracks/Fractures

- Corner pins likely to fail first
  - High stress areas, and corners of the BGA package and die
Solder Balls, Cracks and Fractures

IC / SOC / SiP

Printed Circuit Board

Solder Balls

Typical Failure Points

Fractures

Lall 2005 IEEE
Mechanisms of Failure

- Fatigue fractures (cracks) are caused by thermo-mechanical stress/strain.
- During periods of high stress, fractured bumps tend to momentarily open and cause intermittent faults of high resistance for periods of ns to µs.
- Over time, contamination and oxidation films occur on the fractured faces: the effective contact area becomes smaller and smaller.
- Transient opens can be detected by event detectors.
Mechanics of Failure

HALT results - Pulled FPGA – Damaged Solder Balls

Undamaged

Damaged: Cracked

Cracked

Fractured
Fractures and Intermittency

Vibration flexes components, intermittently opening and closing the circuit.

Intermittent Failure caused by Fractured Solder Joint and Vibrational Stress
Defects: Fractures & Intermittency

High Stress Areas

BGA Package
Fracture
Solder Ball
Multi-Layer PCB

Failure Point: Fracture of the Solder Ball

Intermittent Failure caused by Fractured Solder Joint and Vibrational Stress
Intermittent Faults

- Faults are intermittent: confirmed by CAVE, Auburn Univ., German automobile manufacturer, BAE Systems and other firms
  - Occur during periods of increasing strain
  - Multiple occurrences per cycle
  - Industry standard: 200 ohms +, 200 ns +
Intermittencies

- With present technology, reported electronic system problems in the field cannot be duplicated at the service point or in the lab.

- “Three/Four-letter” words (CND, NTF, RTOK)
  - Could Not Duplicate (CND)
  - No Trouble Found (NTF)
  - Retest OK (RTOK)

- 50 to 80% of these CND/NTF/RTOK problem categories are reported by service personnel.

- Major culprits – Solder joint intermittencies and NBTI effects in deep submicron ICs
Techniques for Interconnect Verification

- X-Ray Laminography
- Analog Harmonic Test
- RF induction & Analog junction technique
- Boundary Scan
- SJ BIST
- Daisy chain of interconnects
Existing Test Methods

- Focus on Manufacturing Process
  - Boundary Scan (JTAG / IEEE 1149.1)
  - Optical / X-Ray Inspection
- Focus on Static Measurements
- Reliability Measurements Are Lacking
  - Reliability = Performance over Time
  - Implies field measurement & monitoring
  - Intermittencies develop after deployment
Limitations of Test Techniques

- **X-Ray Laminography**
  - Typically 98% of all solder joints can be inspected
  - All pins, including power and ground
  - *No info on electrical properties, => cannot detect micro cracks*
  - *Cannot be used for continuity checks*

- **Analog Harmonic Test**
  - Verifies electrical properties of the connection
  - Detects opens & marginal connections (10-20 Ohms)
  - *Requires time consuming learning phase*
  - *Cannot diagnose highly parallel connection arrays, e.g. power/ground nets*
Limitations of Test Techniques

- **RF induction & Analog junction technique**
  - Makes use of the pin protection diodes that need to be biased
  - Detects opens
  - Requires time consuming learning phase
  - Cannot diagnose highly parallel connection arrays, e.g. power/ground nets

- **Boundary Scan**
  - Makes use of logic interaction between connected functional pins
  - Detects Opens & Shorts
  - Can only be used when the circuit is operating in test mode
  - Cannot diagnose highly parallel connection arrays, e.g. power/ground nets
  - No information on degradation
Limitations of Test Techniques

**SJ BIST**

+ Detects opens, shorts and intermittences
+ Runs concurrently
+ Detects degradation and serves CBM approaches
  - Requires dedicated test pins
  - Cannot diagnose highly parallel connection arrays, e.g. power/ground nets
Daisy chain of interconnects

- Detects opens & shorts
- Useful for assembly/soldering process qualification
- Has some diagnosis capabilities
- Useful for HALT testing
- Requires dedicated test pins
- Cannot diagnose highly parallel connection arrays, e.g. power/ground nets
- Requires hard wired connections between pins
Interconnect Daisy Chain
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What is SJ BIST?

- SJ BIST = Solder Joint Built-in Self-Test
  - Original solution enabling the verification and validation of solder joint interconnect reliability
  - Originally developed for FPGA-BGA applications
  - Can be applied to validate the integrity and reliability of any type of interconnection
SJ BIST Objectives & Features

- Objectives
  - Detection of impending interconnect failures
  - Unique in-situ testing in operating circuits
  - Technology-independent

- Feature and Benefits
  - Detects ball fractures prior to catastrophic failure of circuit
  - Provides actionable maintenance data
  - Independently tested and verified
  - Endorsed by leading automotive and aerospace customers
- SJ BIST runs concurrently with host circuit
- SJ BIST requires dedicated I/O
SJ BIST Implementation

- SJ BIST runs concurrently with host circuit
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SJ BIST™ Operation

- Similar to a simple memory test: W0 – R0; W1 – R1
- Runs concurrently with host circuit
- Verilog/VHDL core (patent pending)
  - Each core tests two I/O pins
  - Pins are externally wired together
  - Optionally small capacitor connected to the two pins
SJ BIST Concept

- Interconnect == Memory
  - Connection between two dedicated pins
- Storage element == Capacitance of interconnect
  - Intrinsic (parasitic) capacitance of wire
  - I/O input capacitance
  - Small add-on capacitance
- Test == Transfer Charge == Memory Test
  - Write 0’s and 1’s
  - Verify if 0’s and 1’s are correctly stored
Healthy Solder Joint

Writes a “1” and reads a “1”
Faulty Solder Joint

Writes a “1” but reads a “0”
**SJ BIST Concept**

![ SJ BIST Concept Diagram ]

- C = 10nF,
- R = 1..250 Ohm

Logic 1

Logic 0

V_Cap vs Time (μs)
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Requirement:
Interconnect path dedicated for SJ BIST

On-chip interconnects

Die to substrate (incl. bumps)

Die to board (incl. bumps & balls)
SJ BIST I/O

- **Input (Control)**
  - Clock, Enable & Reset

- **Test Pins**
  - 2 bidirectional I/O pins: TP0 & TP1

- **Output (to host)**
  - Failure Flags (fault was detected on TP0/TP1)
  - Active fault flags (fault is active on TP0/TP1 at the moment of interrogation of SJ BIST)
  - Failure counts (2 8-bit values related to number of faults detected on TP0 and TP1 respectively)
Other SJ BIST Information

- Flags:
  - Permanent vs Intermittent fault
  - Flags can be treated individually or combined in a global Pass/Fail flag
  - Provide “occurrence” information

- Event Counts
  - # of occurrences of a permanent or intermittent fault during a given timeframe
  - Provide “severity” information

- Flags & Event counts are associated with each SJ BIST Test pin
Testing On-chip Interconnect

Need for dedicated on-chip path between SJ BIST™ Observation pins
Testing Die to Substrate
SJ BIST Application

Testing Die to Board

- SJ BIST logic core
- On-chip interconnect metal, vias, contacts
- Bump
- Substrate interconnect
- Substrate
- Ball
- Socket or board interconnect

= Interconnect path being tested
Q: What can SJ BIST HALT™ do for you?

- Thermal Oven with Built-in Shaker (customer-provided)
- Run HALT cycles
- Controller FPGA (customer-provided or opt for Ridgetop’s SJ BIST HALT™ Controller FPGA)
- HALT Board (SJ BIST™)
- Power Supply
- Serial Hub
- SJ BIST HALT™ Program Java
- SJ HALT Analysis™
- Deployment of Most Reliable Solder Process (FPGA-PCB Combination)
Testing Cables
Testing Cables

SJ BIST Core Unit

SJ BIST Connector
SJ BIST Demonstration/Evaluation Kit
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SJ BIST Summary

- **SJ BIST**
  - Detects opens, shorts and intermittences
  - Runs concurrently
  - Detects degradation and serves CBM approaches
  - Serves Process Qualification
  - Serves On-line in-situ Monitoring
  - Serves a wide application range (Package – Board – connectors – cables)
  - Addresses reliability aspects of interconnects

  - Requires dedicated test pins
SJ BIST Summary

- Available as:
  - Verilog/VHDL core
  - Microcontroller code
- Requires dedicated I/O + capacitor
- Runs concurrently
- Interconnect reliability verification
  - Process qualification
  - Lifetime observation
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Questions?

- Slides and recording of the webinar will be available shortly via an e-mail from Ridgetop.

- E-mail follow-up questions & comments to Hans Manhaeve: hans.manhaeve@ridgetopgroup.eu

- Please fill out our brief feedback survey at: https://www.surveymonkey.com/s/PV8N9J8

Thanks for your time and interest!
Thank you!

Ridgetop Group, Inc.

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About Ridgetop Group, Inc.

- Incorporated in 2000, and headquartered in Tucson, AZ. Ridgetop Europe established in 2010 in Belgium.

- Microelectronic Design and Test Solutions:
  - SJ BIST™ Based Test Solutions
  - ProChek™ Semiconductor Characterization System
  - Q-Star Test™ Precision Current Measurement Instruments
  - PDKChek™ In-Situ Test Structures
  - ISO:9001/AS9100C-compliant Design and Integration Services

- Strong market position with commercial and government customers in USA, Canada, Europe, and Asia
Ridgetop maintains a complete Cadence design flow, and has designed circuitry down to the 45 nm process node. Ridgetop also has a line of predesigned and characterized IP blocks that can be used to accelerate the time-to-market for your systems. Examples include precision bandgap references, op-amps, comparators, ADCs, DACs and test structures.

**Our design services include:**

- Analog/mixed-signal and gate array integrated circuits with varying process nodes of 0.5 μm down to 45 nm
- High-speed, high performance, high linearity ADC and DAC design
- Fuel Cell and Battery Management System components
- FPGA-based designs, from basic specification to gate level, with timing analysis and programming
- IP blocks of specialized functionality
- Modeling and simulation
- Completion of back-end design from existing EDIF/SPICE to GDSII layout
- Rescaling “legacy” designs to smaller process geometries
- Radiation-hardened/foundry-specific designs
Q-Star Test

- $I_{DDQ}, I_{DDT}, I_{SSQ}$ and other precision current measurement instruments for characterization and test
- On-board modules and on-chip sensors
- Test and DFT consulting and training services
- 70 semiconductor companies and 700 instruments installed
- Developed by Ridgetop Europe
Q-Star Test Measurement Solutions

- **Static (Quiescent) Current Measurement Instruments** ($I_{DDQ}/I_{SSQ}$)
  - Standard and advanced IDDQ tests
  - Stand-by current measurements
  - Power-down current measurements
  - Bias current measurements
  - Average current measurements
  - Analog DC and low frequency current measurements
  - ....

- **Dynamic Current Measurement Instruments** ($I_{DDT}$)
  - Dynamic and transient (IDDT) current tests
  - Power profiling of circuits and systems
  - Active current consumption
  - E-fuse programming validation
  - ....
Why Ridgetop?

Ridgetop Group Delivers

- Domain Expertise
  (Expansive portfolio of electronic prognostic solutions)
- IP Easily Configured to Target Applications
  (Seamless integration and porting)
- Customer Service
  (Dedicated service and support personnel for on demand assistance)
- Commitment to Innovation
  (Strive to improve/upgrade existing IP)
- World Leaders in Electronic Prognostics
  (Awarded most gov’t contracts)
- World Class Engineering Staff
  (All project contributors PhD or advanced degree)
- IP Easily Configured to Target Applications
  (Seamless integration and porting)
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