ProChek™

The Shortcut to Device and Process Qualification, Characterization, Comparison and Reliability Assessment

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25 June 2015

Agenda

- The Quest for Data – Setting the Scene
- Aspects of IC Reliability
- Degradation Mechanisms of Modern CMOS ICs
- ProChek Concepts
  - Structure and Specs
  - Test Structures: what test structures can ProChek work with
  - How to use ProChek with already existing test structures
  - ProChek TC implementation & application requirements.
- Summary

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The Quest for Data

Macro Issues

- Semiconductor industry business is based on a fabless model
- Foundries share only a limited amount of process information
- Smaller semiconductor structures have relatively more variability in critical process parameters
- Speed and frequency of process changes increases
- Wafer Level Process Monitors have limited statistical significance
- Customers expect ZERO defects on shipped products

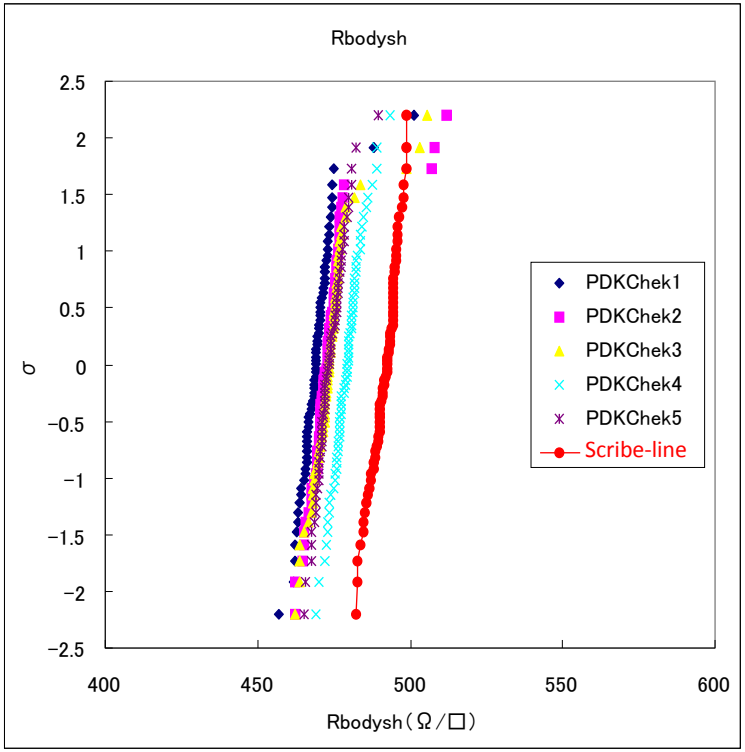
PDK Gaps

- PDK may not be accurate for particular batch/wafer/die/package
- PDK may not have data for particular application (e.g., temp.)
- PDK may not be representative of particular biasing schemes (e.g., MOSFET matching differs for strong inversion and subthreshold)
- Data is not placement specific (proximity/wafer angle)
- PDK may not give values to insert into random parameter fluctuation simulations

In an increasingly cost-conscious and price sensitive landscape, yield loss damage and reliability issues are magnified

The Quest for Data

- Process control monitor (PCM) structures from foundry may not directly measure important parameters
- High performance designs need die-level process monitor (DLPM) results that accurately track actual process tuning



Scribe-line results differ from DLPM results

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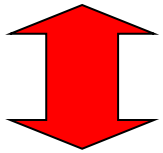
Yield & Reliability

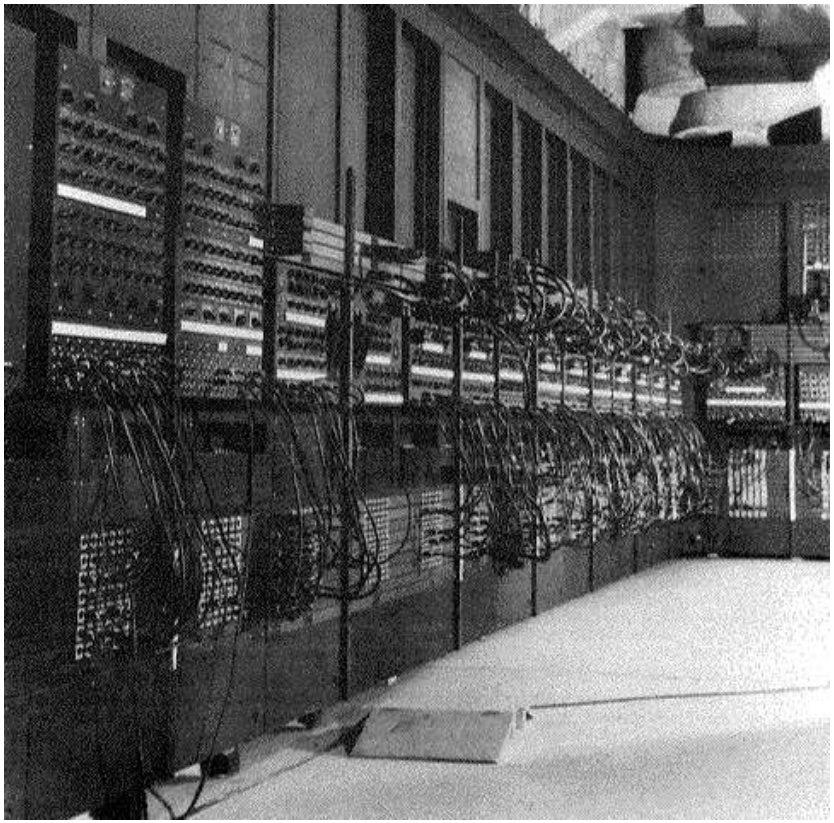
- Semiconductor evolution enables further integration
  - Transistors are nearly free
- New processes are used for mass production long before they are mature
  - Systematic and random defects
  - Reliability concerns
- Increasing device complexity
  - The “embedded” world
  - Analog – Digital – Memory – Software



- Market demands for cheaper and better electronics
- Market demands for RELIABLE electronics

History and Reliability

First “super computer,” 1947 (ENIAC, “the Giant Brain”)

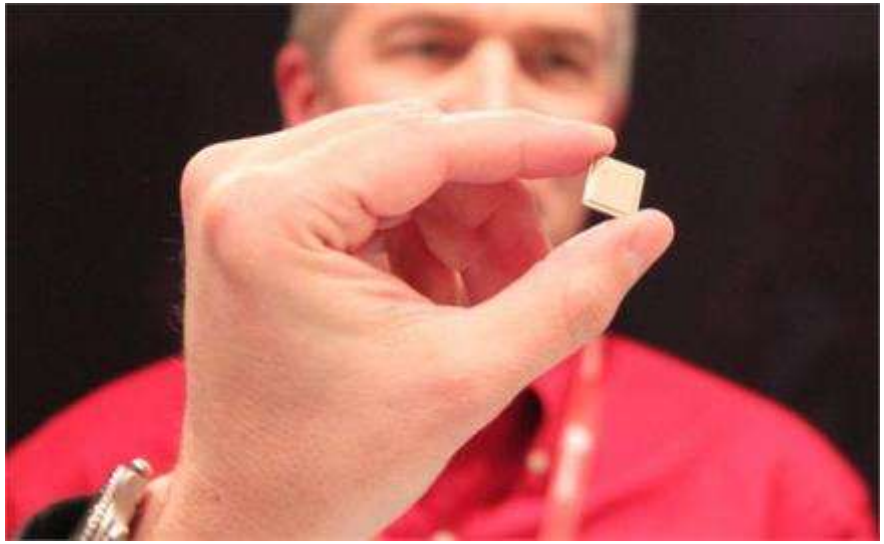


Size: 1800 square feet
Performance: 5,000 FLOPS
Power: 150 kW
Reliability: >10 years

“Where a calculator on the ENIAC is equipped with 18,000 vacuum tubes and weighs 30 tons, computers of the future may have only 1,000 vacuum tubes and perhaps weigh 1½ tons.” – *Popular Mechanics, March 1949.*

Reliability Today

Microprocessor 2012



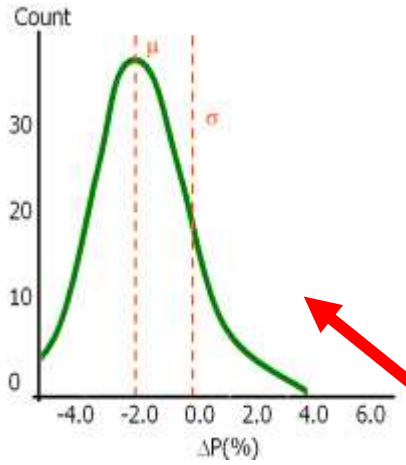
Size: 200 mm^2
Performance: 1,000,000,000,000 FLOPS
Power: 100 W
Reliability: 10 years **???**

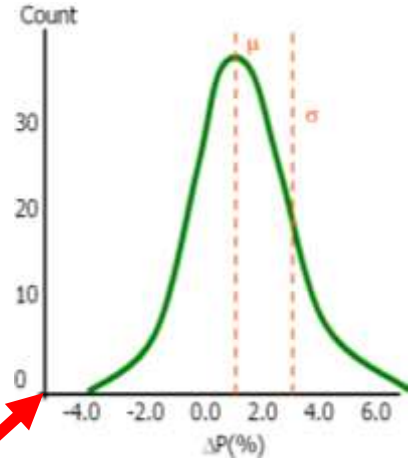
300,000,000,000X improvement in wattage/FLOP in 65 years!

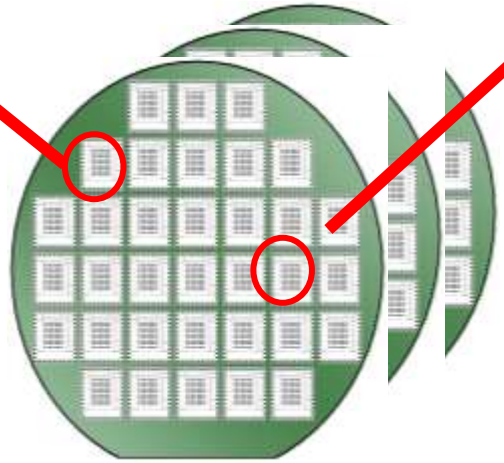
How about reliability?

Need for proper process characterization

Dealing with variance and fluctuations



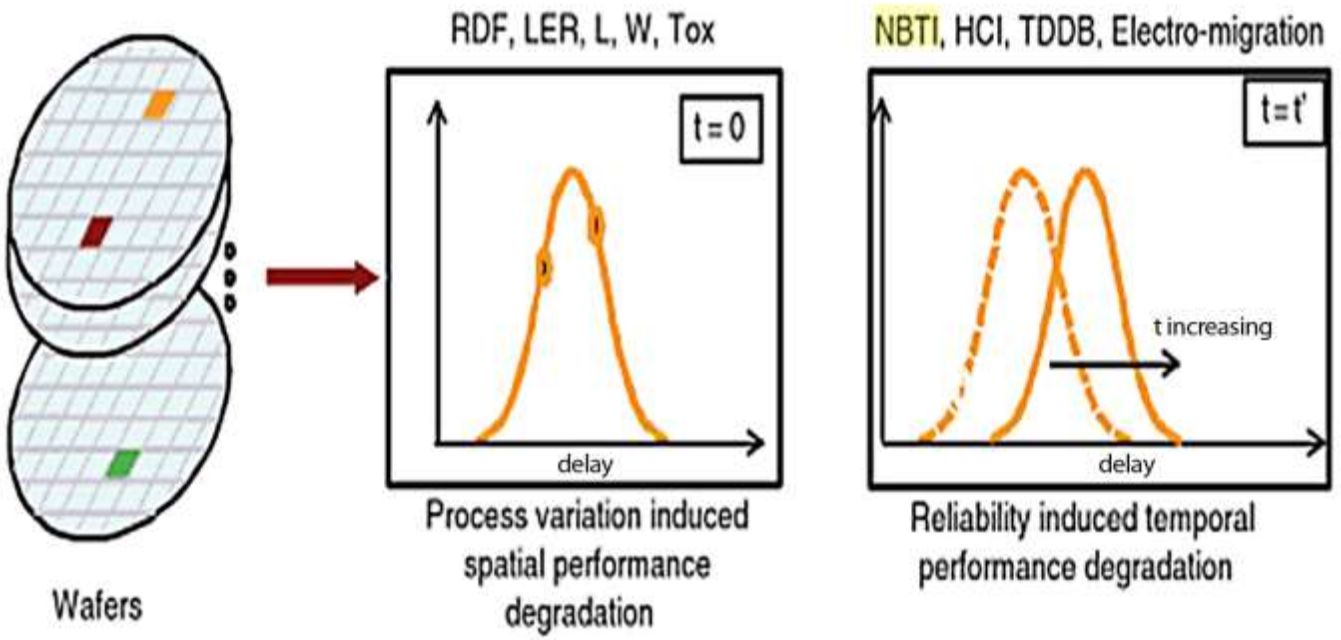




Parameters change across dies, across wafers and across lots

PDK provides the boundaries

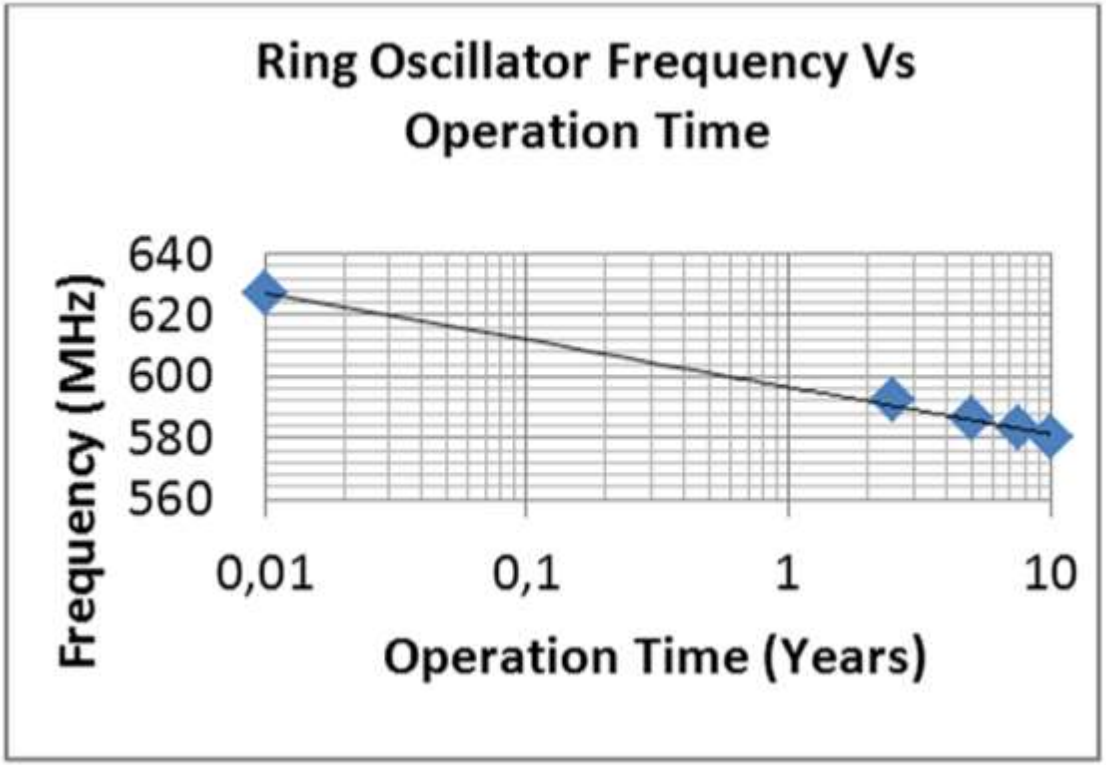
Variability: Impact on Reliability



Time-zero parameter spread due to process mismatch shifts during the operational life due to degradation. Both process mismatch and degradation effects are worse in the smallest-geometry processes.

Source: "Low-Power Variation-Tolerant Design in Nanometer Silicon" By Swarup Bhunia

Aspects of IC Reliability



28 nm CMOS ring oscillator frequency degrades 5.5% within a year in normal operation conditions

Source: Synopsys

Cost of Reliability Problems

B-2 bomber crash in Guam Feb 2008.

- $1.4B loss

Moisture in the transducers during calibration distorted the information in the air data system.

This caused the flight control computers to calculate inaccurate airspeed and negative angle of attack upon takeoff.

http://telstarlogistics.typepad.com/telstarlogistics/2008/08/photos-and-vide.html

Cost of Reliability Problems

SANTA CLARA, Calif., Jan. 31, 2011 – As part of ongoing quality assurance, Intel Corporation has discovered a design issue in a recently released support chip, the Intel® 6 Series, code-named Cougar Point, and has implemented a silicon fix. In some cases, the Serial-ATA (SATA) ports within the chipsets may degrade over time, potentially impacting the performance or functionality of SATA-linked devices such as hard disk drives and DVD-drives. The chipset is utilized in PCs with Intel's latest Second Generation Intel Core processors, code-named Sandy Bridge. … Intel expects this issue to reduce revenue by approximately **$300 million** as the company discontinues production of the current version of the chipset and begins manufacturing the new version. Full-year revenue is not expected to be materially affected by the issue. Total cost to repair and replace affected materials and systems in the market is estimated to be **$700 million**.

Source: Intel Newsroom

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Degradation Effects: Overview

Failure Mode	Physics	System Effect
NBTI (PMOS), PBTI (NMOS)	▪ Negative V_T shift for PMOS, positive for NMOS ▪ Lower leakage and I_{ON}, slower speed	▪ Timing faults in processors other digital circuits ▪ Resettable – but increasing severity over time

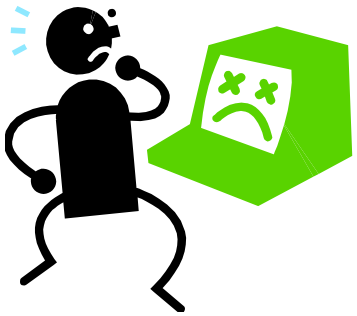
TDDB	▪ Soft breakdown:
	  ▪ Slower speed
	  ▪ Weakened gate oxide
	  ▪ Increased leakage current
		▪ Increased ESD vulnerability
		▪ Non-resettable timing faults

	▪ Hard breakdown	▪ Catastrophic short
Hot Carrier (NMOS)	▪ Positive V_T shift ▪ Change in sub-threshold swing (transistor won't turn OFF)	▪ Increased Off-state power ▪ Increased current draw ▪ Decreased data retention time in DRAM
Metal Migration	▪ Higher resistance in Via connections ▪ Open circuits	▪ Catastrophic open

Overview of the Existing Problem

- Small-geometry fabrication processes are very complex
- Reliability concerns for demanding applications include:
  - Bias Temperature Instabilities
  - Dielectric Breakdown
  - Hot Carrier Effects
  - Electro- / Stress Migration
  - Process Mismatch Effects
  - Lot-to-lot Variation
- For space and radiation-sensitive applications there are also:
  - Single-event radiation effects
  - Total dose radiation effects
- Current techniques are not:
  - Comprehensive enough
  - Accurate enough
  - Fast enough

Our Customers' Problems



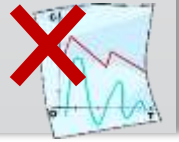
Customer 1:
"Foundries do not give us enough reliability test / process data"

Customer 2:
"We can test only three DUTs in parallel and the test lasts a full month"

Challenges

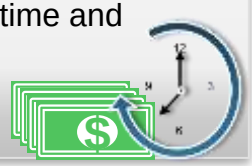
Obtaining Data

- End-User Perspective
  - Incomplete data for reliability analysis
  - May not provide detailed data
  - Does not provide radiation data
- Fab Perspective
  - Expensive and lengthy process to obtain test result data
  - Data Management
    - Several types of data need to be collected accurately
    - Several devices under test (DUTs) are tested at the time



Long & Resource Intensive

- Defining and characterizing semiconductor reliability attributes takes a lot of time and resources.



Expensive Equipment

- Modern test equipment requires a large capital investment, is complicated to use, and may be focused on a single purpose.

Comparative Data

- Selecting the foundry that provides the best performance devices for your products.
- Tracking long term performance and product quality.

Hot Carrier Degradation

Fabs do not give enough reliability test data to designers and reliability engineers

Qual Items	DUT	Structures	Sample size	Stress Conditions	Failure Criteria	Specifications	Result
Gate oxide VBD	1.2V Core	Area = 5e2 ~ 2.4e3 um^2	>=3 wafer/lot; 3 lots; 25,560	Voltage ramp 3.3V/s (inversion mode)	Ig leak > 40uA @ 1V	Do <= 5/cm^2 @ VBD <= 1.2V Do <= 1/cm^2 @ 1.2V < VBD < 2.9V	Pass
	2.5V I/O	Area = 4.8e3 ~ 1e6 um^2		Voltage ramp 6.27V/s (accumulation mode)	Ig leak > 15uA @ 1.5V	Do <= 5/cm^2 @ VBD <= 2.5V Do <= 1/cm^2 @ 2.5V < VBD < 5.0V	Pass
	2.5V I/O over drive			Voltage ramp 6.27V/s (accumulation mode)	Ig leak > 15uA @ 1.5V	Do <= 5/cm^2 @ VBD <= 3.3V Do <= 1/cm^2 @ 3.3V < VBD < 7.2V	Pass
Gate oxide TDDB	1.2V Core	Area ~ 1e7 um^2 (W/L=1/0.06)	>= 50/stress/lot; 3 lots	3-5 stress voltage @ 125C & field ~ 8-12MV/cm	1st soft breakdown	TTF @0.1% cum failure rate > 10yr for 0.1cm^2 @ 125C & 1.2V+10%	Pass
	2.5V I/O	Area ~1e6 um^2 (W/L=4/4.8 x 2000)		3-5 stress voltage @ 125C & field ~ 8-12MV/cm	Hard breakdown	TTF @0.1% cum failure rate > 10yr for 0.01cm^2 @ 125C & 2.5V+10%	Pass
	2.5V I/O over drive			3-5 stress voltage @ 125C & field ~ 8-12MV/cm	Hard breakdown	TTF @0.1% cum failure rate > 10yr for 0.01cm^2 @ 125C & 3.3V+10%	Pass
PID	1.2V Core	W/L=5/0.2	>= 4 wafer/lot; 3 lots	Ig @Vg=1.4Vcc inversion	Ig tailing	Ig tailing < 5%	Pass
	2.5V I/O	W/L=2.63/0.38		Ig @Vg=1.8Vcc (2.6Vcc) for NMOS (PMOS)			
HCI	1.2V Core	W/L=1/0.06	24/pattern/lot; 3 lots	1.2V (Vds=Vgs=1.7V, 1.8V, 1.9V, 2.0V) TTF vs 1/Vds	Idsat change > [illegible]%	DC lifetime > 0.2 yr	Pass
	2.5V I/O	W/L=10/0.28	15/pattern/lot; 3 lots	2.5V (Vds=3.3V, 3.5V, 3.7V, Vgs@Isub(max)) TTF vs Isub^{-m}		AC lifetime > 10 yr	Pass
	2.5V I/O over drive	W/L=10/0.5 (N), 10/0.4 (P)		2.5V (Vds=4.1V, 4.3V, 4.5V, Vgs@Isub(max)) TTF vs Isub^{-m}		0.1% cum failure @25C, Vc[illegible]0% (Core P @125C)	Pass
NBTI	1.2V Core	W/L=1/0.06	>= 20/lot; 3 lots	Vg: 6-9 MV/cm @ 125C; Vs=Vd=Vb=grounded	Idsat degrade > 10%	TTF 0.1% cum failure @125C, Vcc+10% >5 yr	Pass
	2.5V I/O	W/L=10/0.28					
	2.5V I/O over drive	W/L=10/0.4					
EM	M1 + contact	W/S=0.09/0.09 (1800 A)	> 20/pattern/lot; 3 lots	Jstess=1-5MA/cm^2 @ 300C	dR >10% Ro	TTF 0.1% cum failure @110C > 100k hr	Pass
	Mx + Vx	W/S=0.10/0.10 (2200 A)					
	My + Vy	W/S=0.20/0.20 (5000 A)		Jstess=1-5MA/cm^2 @ 350C			
	Al-Cu RDL	W/S=3/2 (14.5K A)		Jstess=1-5MA/cm^2 @ 250C			
SM	Vias chain	metal-via overlap from min to 0.7	>130/lot; 3 lots	500 hr bake @175C	dR >10% Ro	No failure allowed	Pass
IMD Low-K TDDB	M1, V1, M2 combs	M1 & M2 W/S=Min/Min V1 W/S=0.10/0.13	>30 /pattern/lot; 3 lots	2.5-4.0 MA/cm @ 125C	I(TBD) = 100 x I(T=0)	TTF 0.1% cum failure @125C & 3.6V > 10 yr	Pass

DC lifetime for Hot Carrier >**0.2 yr**, AC lifetime >**10 yr** in a 65 nm CMOS process

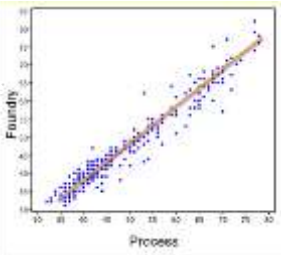
http://www.siliconbluetech.com/media/downloads/SBT_65LP_Process_Qual_v0.1.pdf

Characterization Systems Should…

Deliver lots of data

- Quickly
- Accurately & repeatable
- For different devices
- For different operating conditions

Be inexpensive to own and operate



Allow for direct correlation across foundries and processes

Be easy to use

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What is ProChek ?

An innovative low-cost concept serving to rapidly

characterize intrinsic process reliability and monitor process quality

ProChek…

- Is a flexible & dedicated semiconductor qualification and reliability characterization system.
- Is based on a cost-effective bench-top instrument.
- Interfaces to a variety of test structures
  - Single devices
  - Wafer level test structures
  - Dedicated test chips.
- Accelerates testing of semiconductor devices in volume.

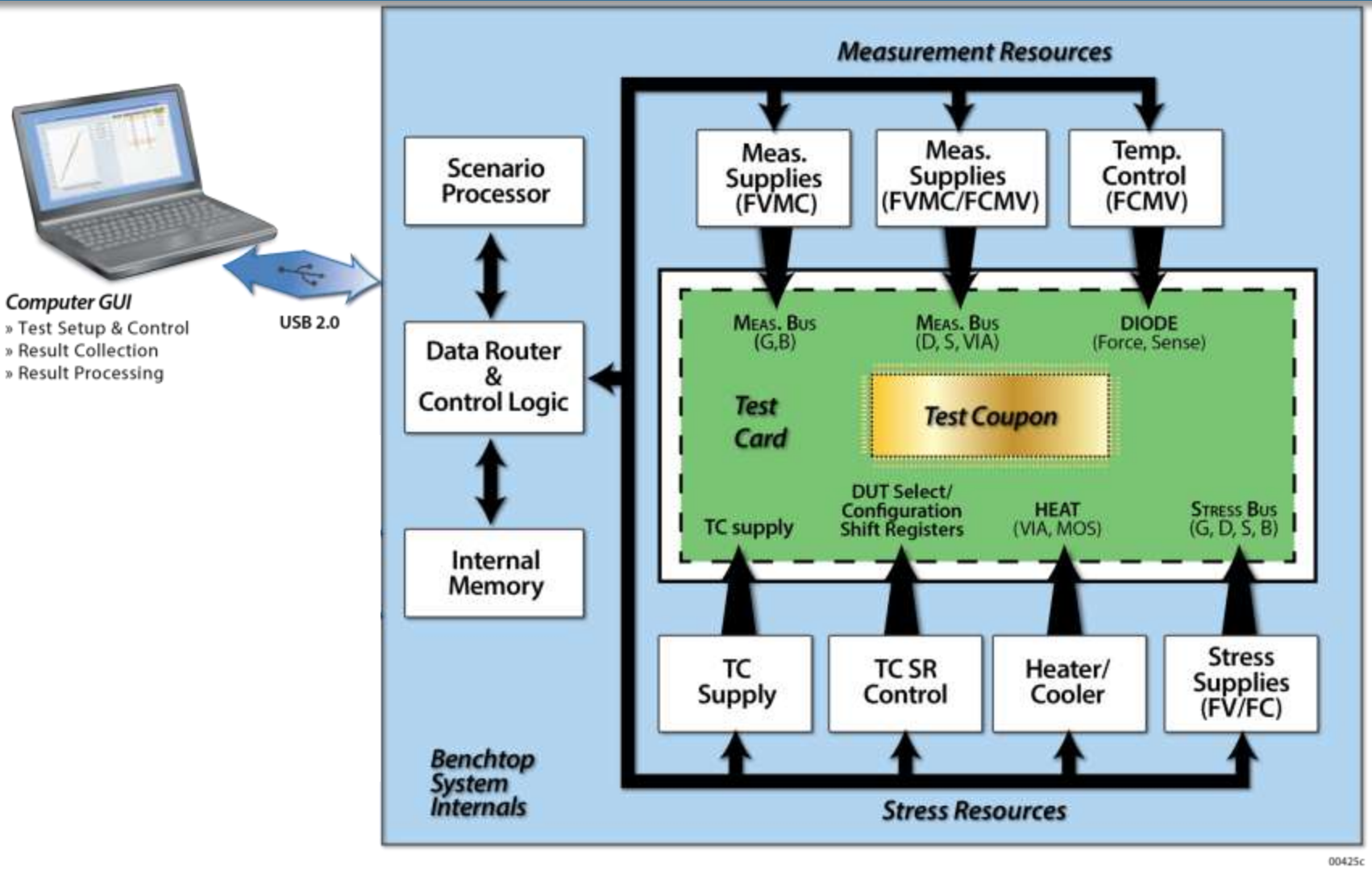
Why ProChek

- ProChek serves to
  - Characterize/quantify existing and new processes from a quality/performance perspective
    - → gather device data (I/V curves, point measurement data)
  - Characterize/quantify existing and new processes from a reliability perspective
    - → evaluate performance degradation over time in function of operation and stress conditions

ProChek Concept

- Analogy: Orchestra
  - ProChek resources == musical instruments
  - Scenario processor == Conductor
  - Test Strategy == Music piece
  - User == Composer
    - → Controls how the music is played (key, timbre, …)
    - → Can write his own partitions

ProChek Benchtop Tester Architecture



ProChek Base Line System Resources

- ProChek offers full 4-terminal (gate, drain, source, body) control
  - Resources:
    - → 4 Stress resources, serving to apply electrical stress
      - can operate in Force Voltage (FV) or Force Current (FI) mode
    - → 4 SMUs, serving to collect data
      - can operate in Force Voltage Measure Current (FVMI) or in Force Current (FI) mode,
      - 10µs sampling, 4K data buffer per instrument, 24bit data
    - → Voltmeter
      - Can operate in absolute or differential mode
      - Can operate as “slow” (10µs sampling) or as “fast” (500ns sampling) meter
    - → Utilities
      - Utility Voltage source
      - Utility Current source
      - Utility Voltmeter
      - Heater/Cooler control

ProChek Extensions

- ProChek has provisions for expansion with additional (add-on) instruments.
- User specific test structures can easily be converted to a native ProChek test structure by means of an active interface board.

- A new ProChek platform supporting up to 24 (48) instruments/SMUs goes to beta Q3-2015

Application Requirements

- ProChek System
- Device under Test (DUT) or a set of DUTs
- Interface to link DUT with ProChek system
  - Function of DUT nature (packaged, wafer structure, set of DUTs)
    - → Simple cable with appropriate connectors
    - → Passive Adapter/interface board with DUT socket
    - → Active interface board with DUT socket
    - → Probe card + link between probe card and ProChek system

ProChek Test Coupon

What

- Combination of test structures, switch matrix and control logic
- Similar test structures are grouped in blocks
- Test structures in a block are stressed concurrently and measured individually

Existing test structures

- Wafer level or packed structures
- Combined with an active interface board

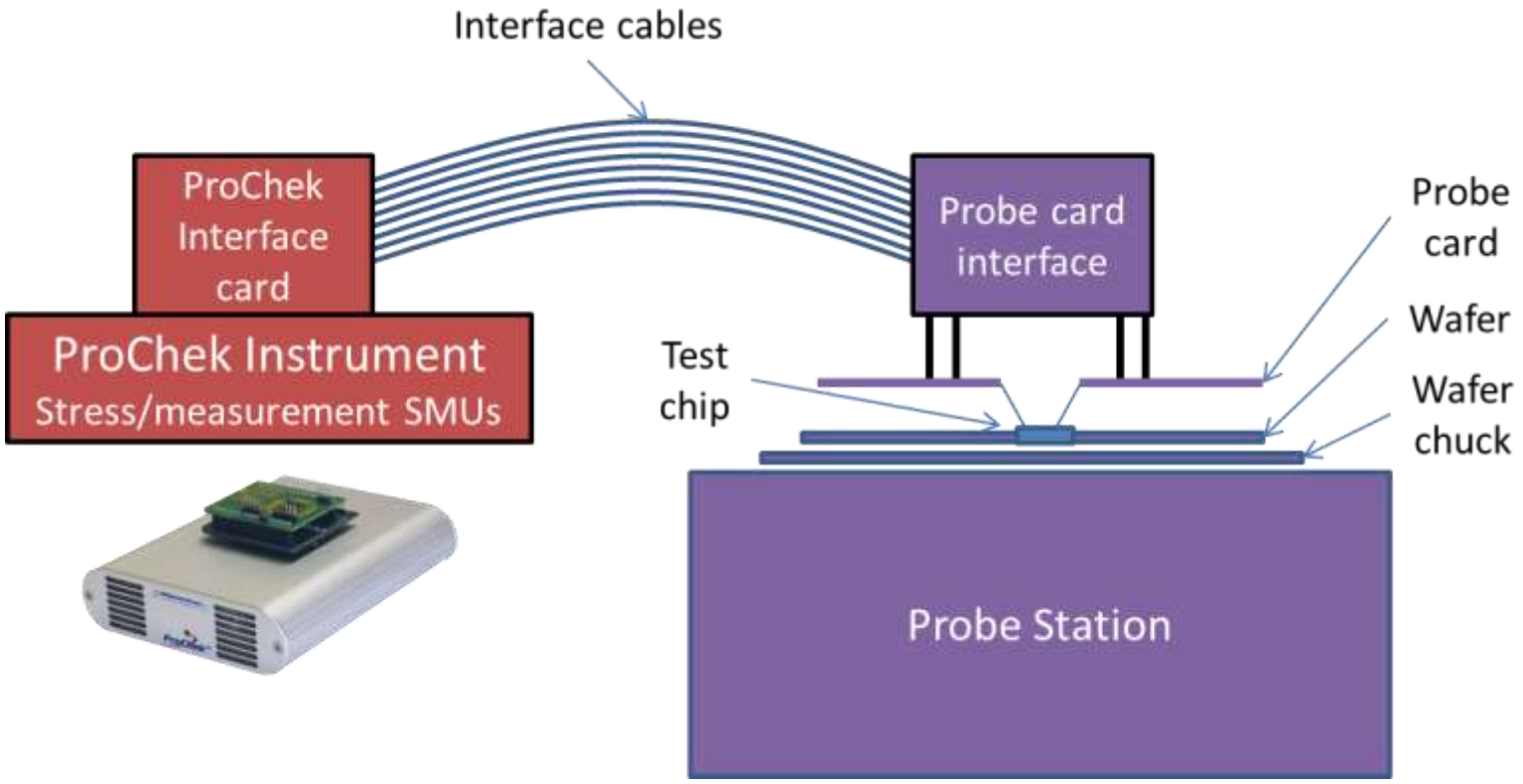
Dedicated ProChek Test structure

- Integrated Single chip containing test structures, stress features and control circuitry
- Multi-chip solution

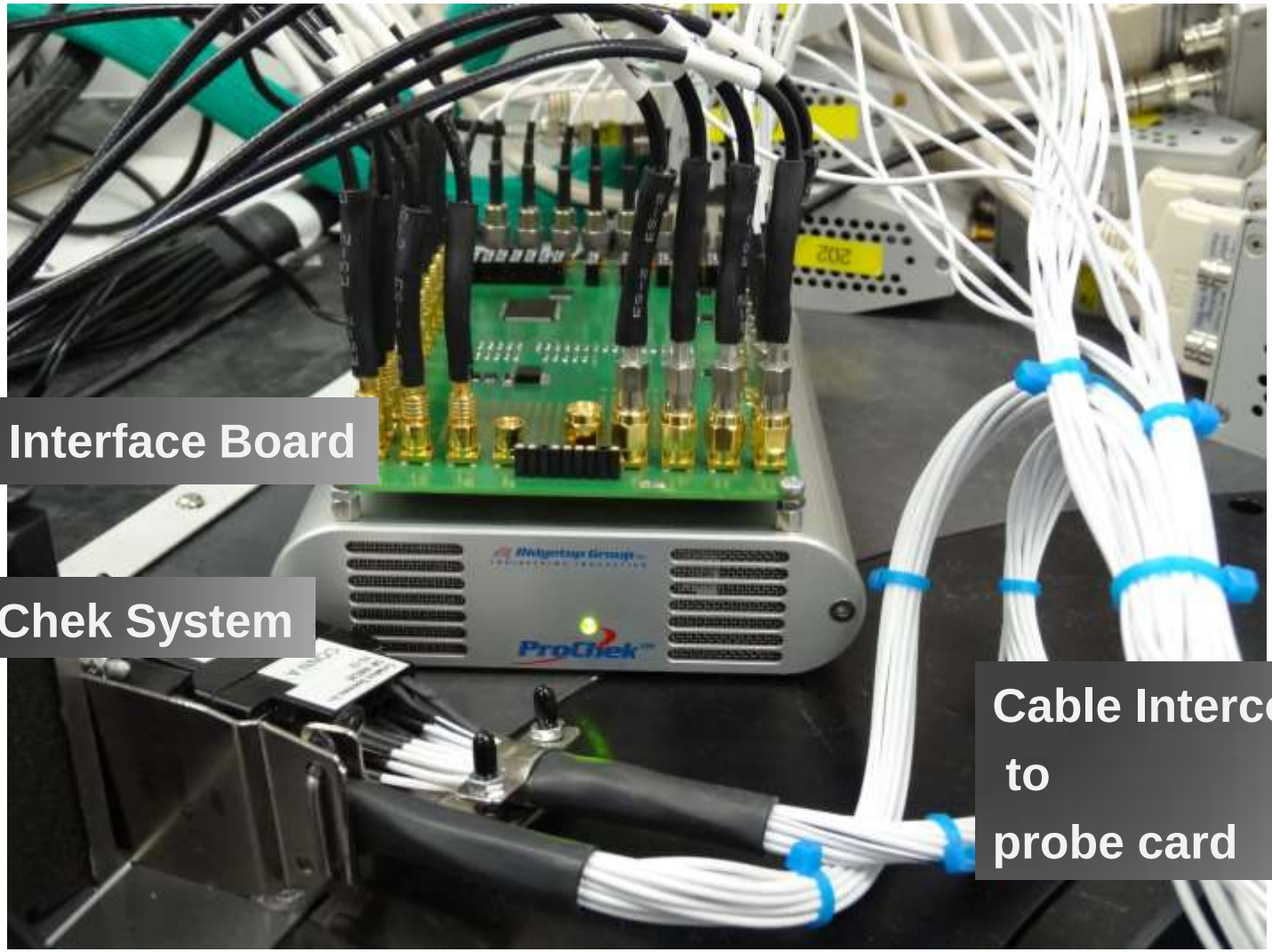
ProChek Interfacing

- ProChek interfaces with
  - Wafer Level structures
    - → Probe card + cable or direct docking
    - → Probe card + smart interface board
  - Packaged devices
    - → Interface board (with sockets)
      - Simple (basic interconnect)
      - Smart (interconnect + selection functionality)
  - …

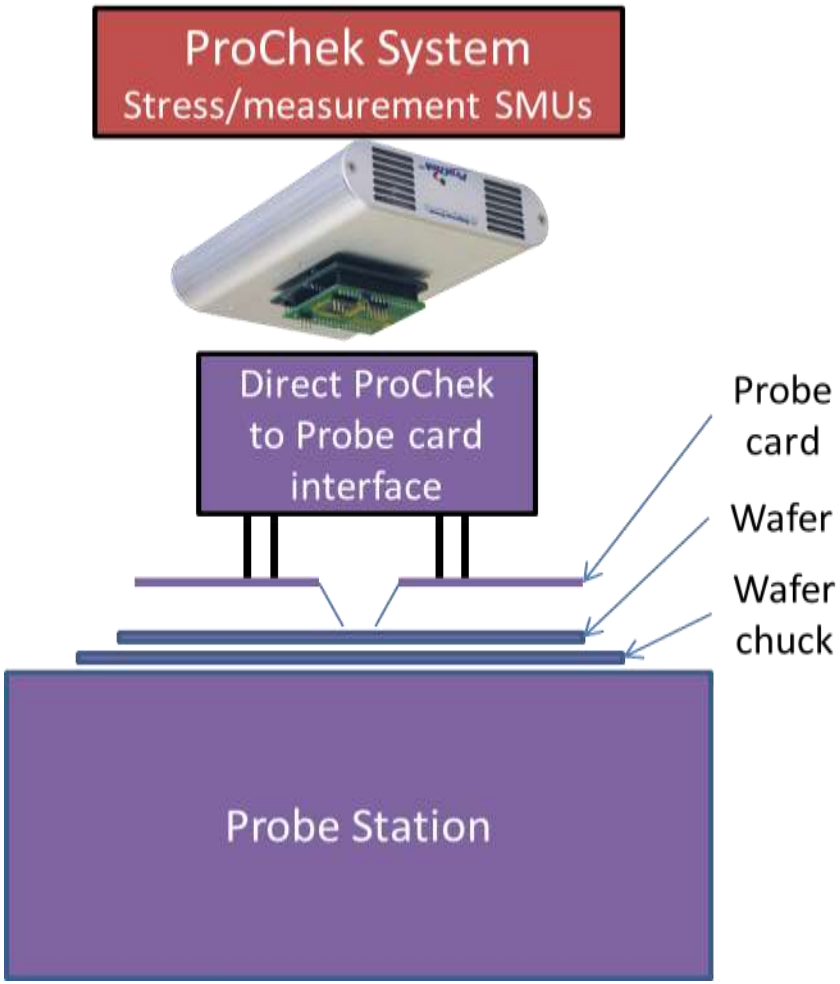
ProChek Application



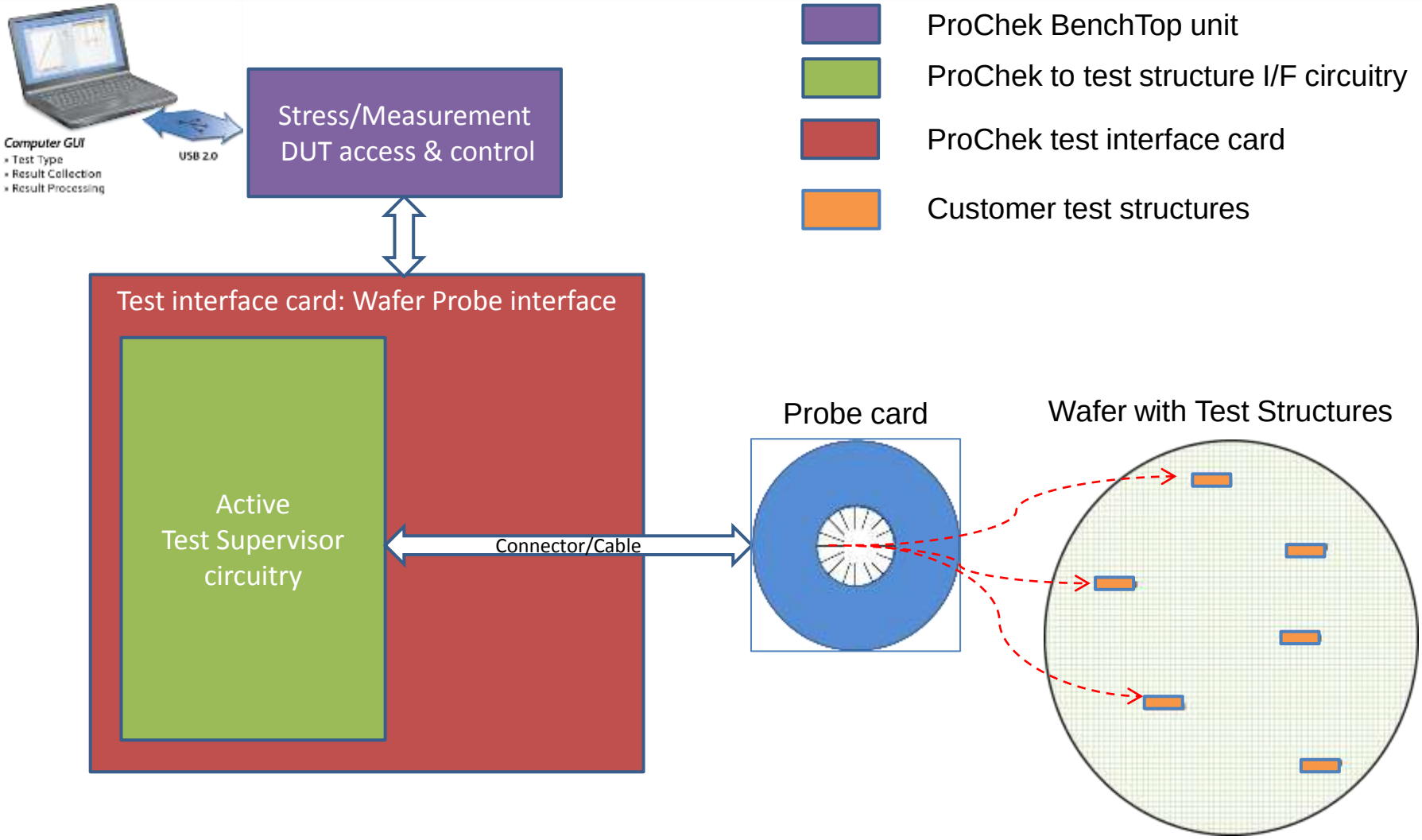
Example – Probe application



ProChek Application



Customized Wafer Probe Interface



Customized Package Interface

Stress/Measurement
DUT access & control

Test interface card: Wafer Probe interface

Active
Test Supervisor
circuitry

Packaged
Test
structure

Packaged
Test
structure

ProChek BenchTop unit

ProChek to test structure I/F circuitry

ProChek test interface card

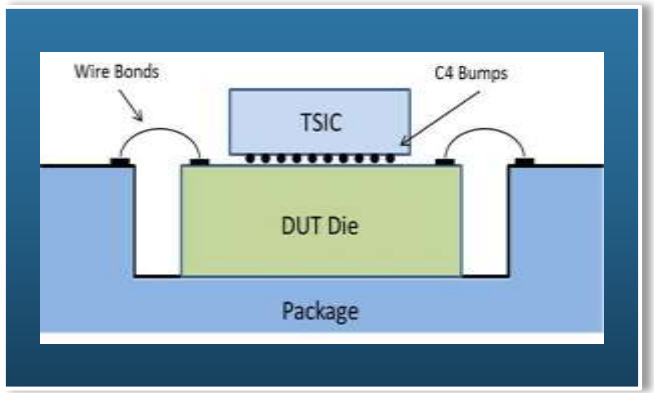
Customer test structures

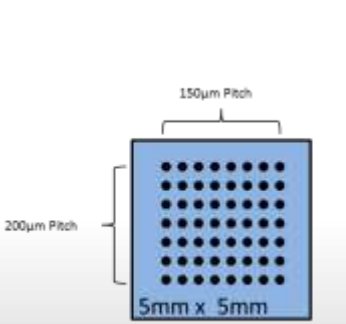
One (or more)
packaged devices
with
Test Structures

Types of ProChek Test Coupons

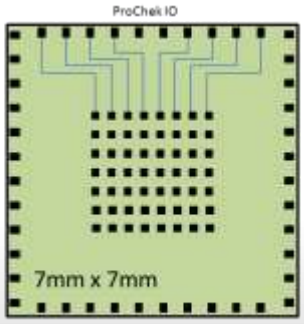
Multi-chip solution: Test Supervisor IC + DUT IC

- A combined Test Coupon solution consists of a Test Supervisor IC (TSIC) and one or more DUT ICs.
- TSIC:
  - Contains Control and Switching matrix
  - separate die in a mature, higher voltage process.
- DUT IC:
  - DUT structures and heaters
  - separate die using the process of interest.
- The two dies are combined in a single package.





TSIC- High Voltage CMOS

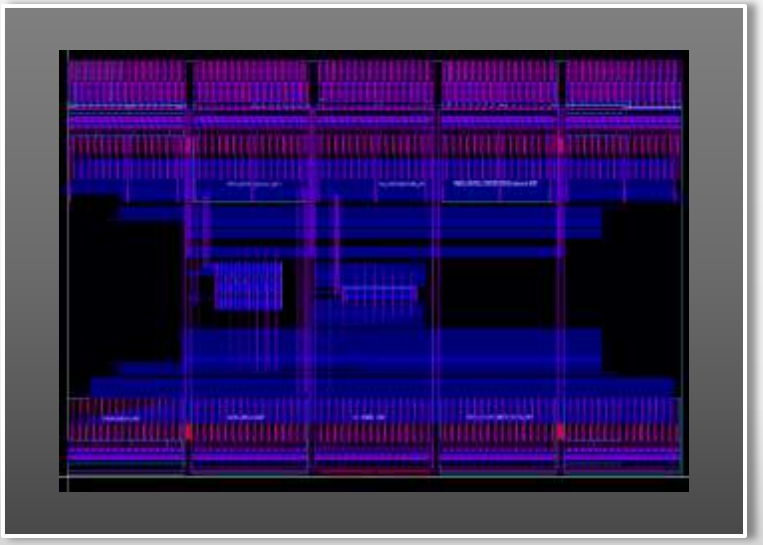


DUT IC – Process of Interest

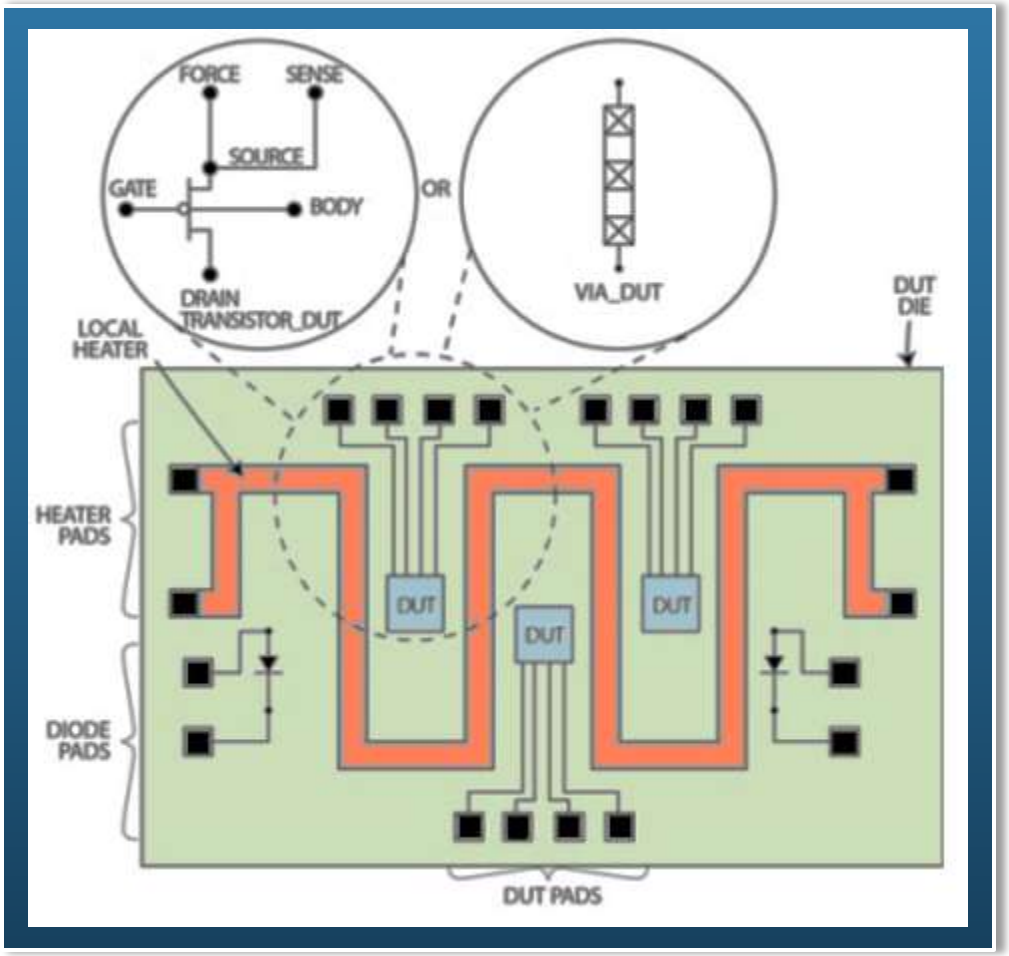
Types of ProChek Test Coupons

Integrated Test Coupon

- DUT test structures, control, selection logic, switches, and heaters on a single die.
- Requires both:
  - “Mature”, well defined process, for which there is a stable and well-qualified PDK
  - Process featuring more robust transistors than the DUT test structures



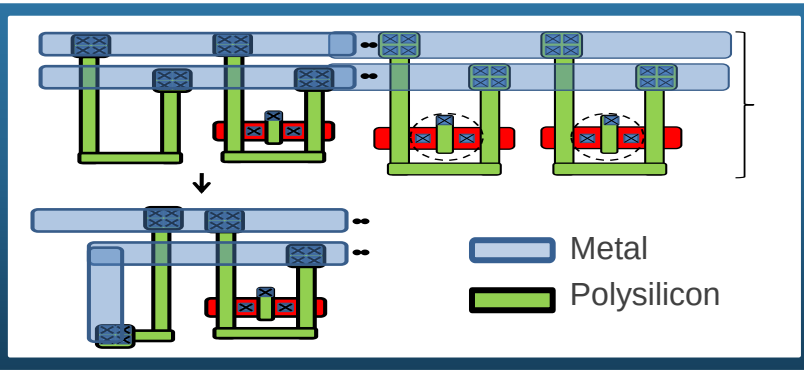
ProChek DUT IC

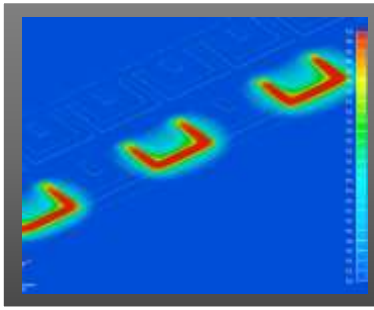


- ProChek DUT IC has an array of DUTs (e.g., transistors, vias) with all terminals padded out.
- Local heaters and temperature measurement diodes are optional.
- One DUT IC typically contains 16 blocks with 8 DUTs of the same type per block
- On-chip local resistive heating elements can be used to significantly increase degradation rate.

Local Heating Structures

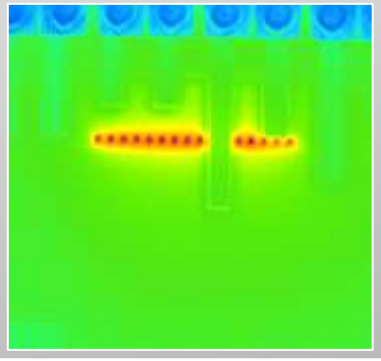
- Polysilicon tracks are used to create a border around each DUT.





- Localized DUT heaters reach maximum temperature in milliseconds. Non-stressed structures do not undergo any damage.
- Current is forced through these resistive elements to heat the area around the DUTs to over 300 ºC.

- Infrared camera data from embedded heating test from IBM 8HP test coupon
- Increasing temperatures will reduce EM, SM and BTI test time and cost



Built-In Test Scenario Descriptions

Charge to Breakdown – QBD [MOS transistors]

- Gate Current [Ig] is measured against Gate Voltage [Vg] during a destructive ramp of Vg.
- DUTs are tested until oxide breakdown and device destruction.

Time-Dependent Dielectric Breakdown – TDDB [MOS transistors]

- Ig is measured for a DC bias of Vg.
- DUTs are measured at a programmable frequency, duration, and test temperature.

Hot Carrier Injection – HCI [MOS transistors]

- Drain-Source Current & Voltage [Ids, Vds], and Ig are measured for a DC Bias or DC sweep of Drain and Gate terminals.
- DUTs are measured at a programmable Vds,Vgs sweep parameters, frequency, duration, and test temperature.

Built-In Test Scenario Descriptions (cont.)

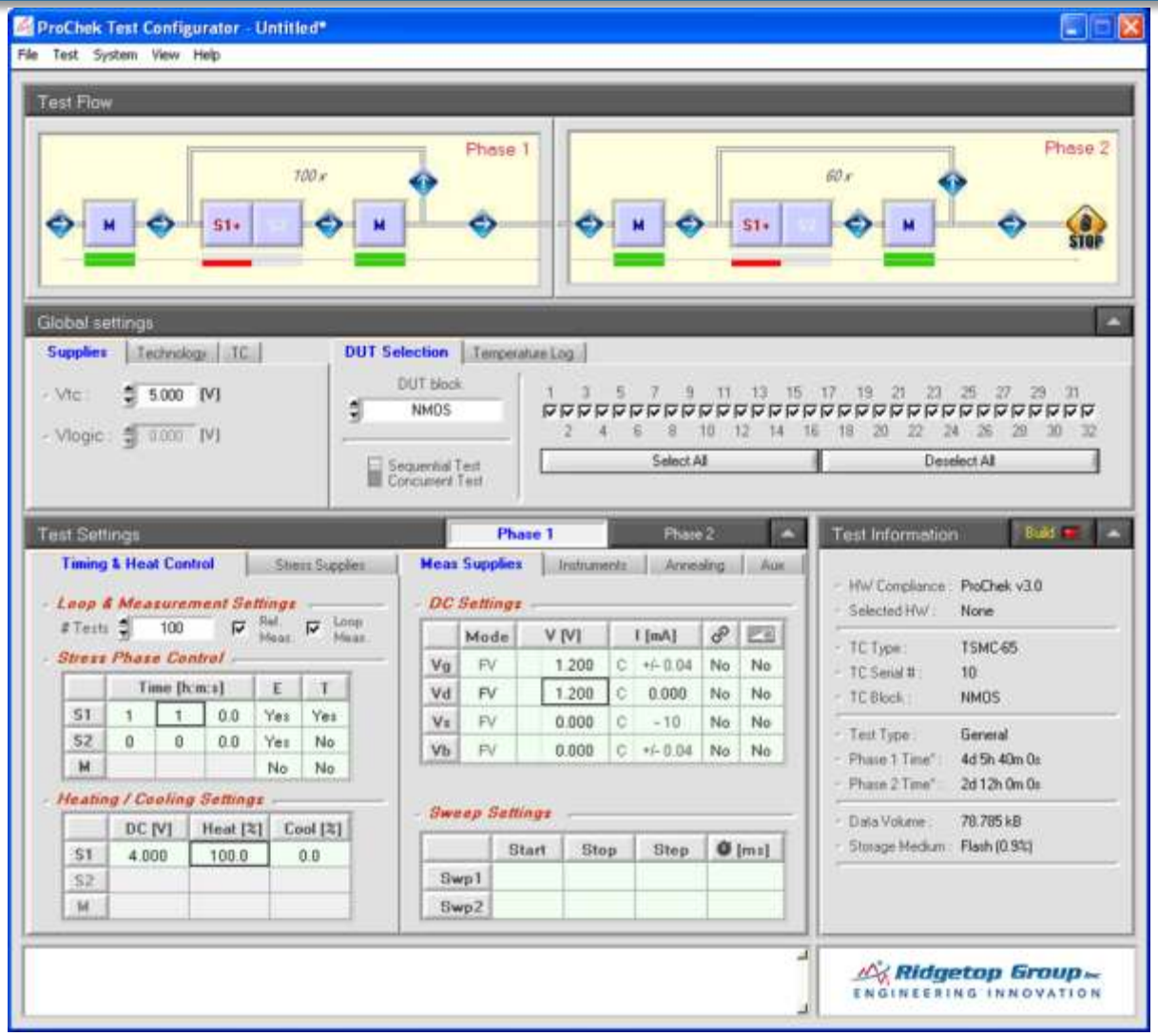
Bias Temperature Instability – BTI [MOS transistors]

- Ids, Vds, Ig, and Body Current [Ib] are measured for a DC Bias or DC sweep of Drain and Gate terminals.
- Fast annealing observations are available to capture Fast-BTI effects.
- Tests include Stress phase and Relaxation phase to observe stress accumulation and relaxation.
- DUTs are measured at a programmable Vds,Vgs sweep parameters, frequency, duration, and test temperature.

Via Electromigration & Stress Migration – VIA EM/SM [vias &metal structures]

- Vds and Ids are measured for a DC bias of the Drain-Source terminals.
- DUTs are measured at a programmable frequency, duration, and test temperature.

ProChek Software Interface

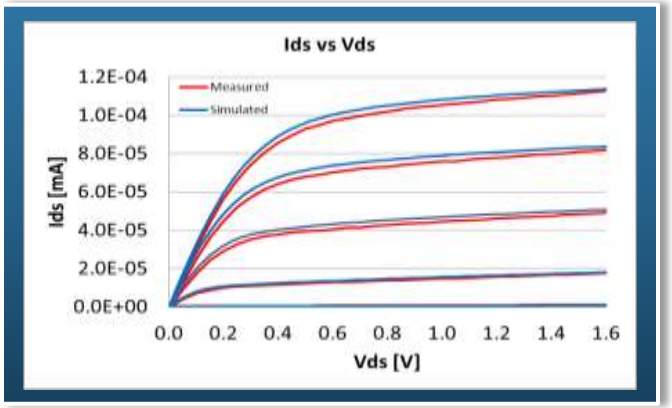


Application Advantages

- Serves to independently validate foundry data
- Serves to collect transistor characterization that is more relevant to design goals than the standard test structure data provided by the foundry by supporting using design specific test structures and using design specific operating conditions.
  - Difference to basic foundry data:
    - → Different transistor dimensions supported
    - → Different operating conditions
    - → Track process and get real data on actual process optimization
    - → Investigate yield issues
      - Options for yield software “YieldMaxx™”
    - → Better device binning

Foundry PDK May Not Be Sufficient

Reliability Concerns	Foundry PDK	ProChek
Variations Across Wafers & Lots		■
Application-specific effects (e.g., temperatures, radiation, biasing, specific geometries)		■
Physical fabrication effects (e.g., directional, wafer angle)		■
Random parameter fluctuation simulation data		■



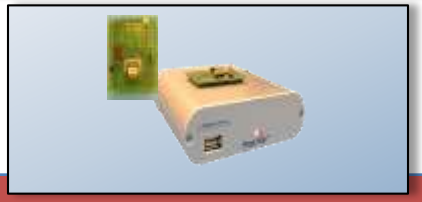
Optional capabilities

- General Instruments “Plug and Play”
- Ring Oscillator evaluation
  - ProChek can drive RO structures oscillator (operating voltage)
  - ProChek can be extended with an instrument to measure RO frequency and perform voltage/frequency analysis.

ProChek Advantages

- Small test platform
  - Replaces rack & stack equipment
- Easy application
- Reliable high precision instruments
- Fast data gathering
- Flexible in use
- Can run full transistor characterization
- Can deal with simple as well as complex test structures
- Supports Yield learning

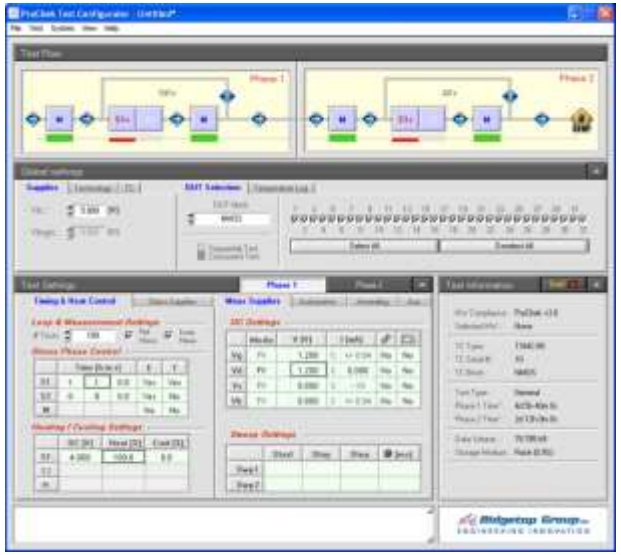
ProChek vs. Competition



Feature	"Rack & Stack"	Other reliability Characterization Systems	ProChek
Application breadth	Specialized instruments and cabling required.	Specialized optional modules required.	All-inclusive (NBTI, TDDB, HCI, EM/SM)
Measurement quality	Repeatability difficult.	High quality; lengthy measurement paths.	High quality, easily repeatable.
Test acceleration	Handful of DUTs in parallel. Requires external ovens or heated chucks.	Moderate number of DUTs. Requires external ovens or heated chucks.	Many hundreds of DUTs per test coupon. One PC supports multiple benchtop units. Embedded heaters.
Ease of Use	Complicated test development and application. Changeover difficult.	Simplified usage model. Changeover can be difficult.	Highly intuitive usage model. Changeover = unplug one card, replace with another.
Size & environment	One or more instrument racks + bench. Controlled environment advised.	Multiple instrument racks. Controlled environment needed.	Any lab, fab or office. Size = ~ paperback novel.
Cost	~$140K acquisition. Hard to maintain.	~$400K acquisition. Moderate maintenance, large floor space.	~$65 acquisition. Minimal maintenance, no floor space.

Additional ProChek Benefits

- Independent characterization of advanced semiconductor processes.
- Characterize non-standard transistor structures (various W/L, enclosed gates, enclosed drains)
- Accelerated characterization of new and existing processes
- Statistically significant and accurate process quality information
- Low total cost of ownership
- Small, portable, and easy to User Interface (UI)



Summary

ProChek

Advanced, dedicated system for fabrication process characterization offering significant advantages to IC designers, process, and reliability engineers.

- Covers reliability concerns of modern nanotechnology processes, including radiation effects (via RadChek)
- Covers qualification needs for new and immature processes
- Significant cost and time savings

Questions?

- Slides and recording of the webinar will be available shortly via an e-mail from Ridgetop
- E-mail follow-up questions & comments to Dr. Hans Manhaeve at hans.manhaeve@ridgetop.eu
- Please fill out our brief feedback survey at: https://www.surveymonkey.com/r/TMQCNHP

Ridgetop Group, Inc.

Ridgetop Group Facilities in Tucson, AZ

- Arizona-based firm, founded in 2000, with focus on electronics for critical applications
- Two divisions: Semiconductor & Precision Instruments (SPI) and Advanced Diagnostics & Prognostics (ADP)
- Technology leader in precision test structures for QA and prognostic applications
- Wide range of commercial and government customers

- Worldwide nanotechnology R&D partners in industry and academia
- Foundation and focus in physics-of-failure for electronic systems

Ridgetop Europe Facilities in Brugge, Belgium

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