Testing and Design-for-Testability Solutions for 3D ICs

The Hype, Myths, and Realities

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Outline

• Technology Overview
• Hype, Myths, and Reality
• 3D IC Test Challenges
  – What to test? When to test? How to test?

• Emerging Solutions
  – Recent advances
  – Some controversies
Stacking with Through-Silicon Vias (TSVs)

**Traditional stacking with:**
3D chip stacking with wire-bonds:
Heterogeneous technologies
Not-so-dense integration, Not-so-small footprint

**New stacking technology:**
Through-Silicon Vias (TSVs):
Metal vias that provide interconnects from front-side to back-side through silicon substrate

<table>
<thead>
<tr>
<th>Diameter</th>
<th>5 µm</th>
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<tbody>
<tr>
<td>Height</td>
<td>50 µm</td>
</tr>
<tr>
<td>Aspect ratio</td>
<td>10:1</td>
</tr>
<tr>
<td>Minimum pitch</td>
<td>10 µm</td>
</tr>
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</table>
Applications

Memory-on-Logic (JEDEC Wide I/O DRAM)

- 4 channels (a-c)
- 4 x 128 bit = 512 bit I/O
- 4 x 4.25 Gbytes/s = 17 Gbytes/s bandwidth
- Up to 4 stacked dies (Rank 0-3)
Future applications:

- Logic-on-logic
- Multi-tower stacks (both logic-on-logic and memory-on-logic)
Difficult to process wafers thinned below 100 microns

- Mount wafers on temporary wafer handlers (carriers)
- Thinning and backside processing

Option 1: Mount IC wafer face-down on carrier, bond “face-up” (B2F)
  - Scalable solution, supports more stacked layers

Option 2: Bond wafer to 3D stack in “face-down” configuration (F2F)
  - More interconnects between active device on two layers
  - Number of stacked dies limited to 2
Fabrication of IC Stacks

**IC Tier 1**
- Aligned F2F bonding
- Thinning
- F2F

**IC Tier 2**
- Temporary bonding
- Thinning
- Aligned B2F bonding
- B2F

**Face**
- Back

**Carrier Wafer**
Steps in F2F Bonding

- Align
- Bonding
- Thinning (grinding)
- Backside via and bump process
Steps in B2F Bonding

1. temporary carrier bonding
2. back-side thinning
3. expose Cu nails
4. permanent bonding
5. temp, carrier de-bonding
Hype: Industry Trends in 3D Integration

3D-IC Reference Flow: CoWoS

TSV process for narrow pitch: 10µm

20nm technology with TSVs

About to stack DRAM on Volta GPUs

Research in 10µm-pitch micro-bumps

€25M investment for in-house production of 3D ICs
Hype: Industry Trends in 3D Integration

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Hype: EDA Support for 3D Flows

- Tools for 3D included in TSMC Reference Flow
- Validated on a memory-on-logic design with Wide-I/O DRAM
- Collaborates with A*STAR IME to Optimize Through-Silicon-Interposer (TSI) Technology
3D ICs: Reality

- 3D stacking technology demonstrated on silicon (but limited)
  - Xilinx, TSMC, GlobalFoundries, AMD

- Cost remains ultimate challenge

- Efficient 3D IC ecosystem needed for high-volume manufacturing
3D ICs: Reality (AMD “Fiji”)

First high-volume interposer
First Through Silicon Vias (TSVs) and 
μBumps in the graphics industry
Most discrete dies (22) in a single package
Total 1011 sq. mm.
186k μBumps, 25k C4 bumps

4GB High-Bandwidth Memory
4096-bit wide interface
512 Gb/s Memory Bandwidth

Graphics Core Next Architecture
64 Compute Units
4096 Stream Processors
596 sq. mm. Engine

Jeff Rearick, 3D Test Workshop, 2015
Reality: Need for 3D IC Ecosystem

- 3D tools
- 3D partitioning
- Floor planning
- Interface standards: Wide I/O, test I/O
- 3D tools
- Libaries
- PDKs
- Ref. flows
- Cost models
- Test strategies

[source: cadence.com]
Reality: Supply Chain Needed
From Two to Three (or More?) Test Insertions

Known Good Die (KGD) test

Known Good Stack (KGS) test

2D Flow
- wafer fab
- wafer test
- assembly & packaging
- final test
- Pre-Bond Wafer Test
  - KGD for stacking
  - ATE + wafer probe station

3D Flow
- wafer fab 1
- wafer fab 2
- wafer fab 3
- pre-bond wafer test 1
- pre-bond wafer test 2
- pre-bond wafer test 3
- 3D stacking
- post-bond wafer test
- assembly & packaging
- final test

Test Content, Test Delivery, Test Resource Optimization and Reuse (Cost Minimization)
3D Test Challenges

- How to test the interposer?
- Micro-bump probe access
  - Probe needles much larger than TSV/micro-bump size and pitch
- Probe card applies force (weight)
  - TSVs/microbumps have low fracture strength
- Post-bond access: No direct access to non-bottom dies
- New defects due to TSV manufacturing process

[IMEC]
TSV Defect

- **How to test the TSVs? Pre-bond, post-bond**
  - Underfill, pinhole defects, opens: pre-bond
  - Misalignment, mechanical/thermal stress: post-bond thermal effects

**Examples of TSV Defects** (IMEC, Belgium)
TSV Defects

(a) – Fault-free TSV
(b) – Resistive-open defect
(c) – Leakage defect
**TSV Defects (Contd.)**

**Stress-induced defects**
- Copper area
- Silicon area
- Overall area

<table>
<thead>
<tr>
<th>Cu - area</th>
<th>Si - area</th>
<th>Overall area</th>
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</thead>
<tbody>
<tr>
<td>Thermal mismatch (extrinsic stress)</td>
<td>Rapid grain growth (intrinsic stress)</td>
<td>Bump process-induced stress</td>
</tr>
<tr>
<td>▪ TSV extrusion</td>
<td>▪ Void formation</td>
<td>▪ Plastic deformation &amp; fracture in bump and soldering</td>
</tr>
<tr>
<td>▪ Debonding</td>
<td>▪ Void growth &amp; coalescence</td>
<td>G. Lee et al – 3DIC'12</td>
</tr>
<tr>
<td>▪ Bump crack &amp; delamination</td>
<td>▪ Crack generation &amp; propagation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ Cu-induced residual stress</td>
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Pre-Bond Testing of TSVs: Myth or Reality

• Some semiconductor companies say no!
  – Too fragile, too difficult to test pre-bond
  – Process people will fix the yield problem!
  – “We deal with much larger number of vias through DFM rules, and TSVs are at least an order of magnitude larger…”

• But…
  – TSV defects affect surrounding silicon!
  – So more testing of die logic needed
  – Micro-bump defects not addressed as easily by process fixes
  – Probing solutions on the horizon
Cascade Microtech’s Probe Technology

- Pyramid Probes® Rocking Beam Interp.
- MEMS-type thin-film probe card
- Lithographically-defined probe tips

IMEC’s 2.5D Test Chip ‘Vesuvius-2.5D’

- Full four-bank JEDEC Wide-I/O interface (= 1,200 micro-bumps)
- Daisy-chains through micro-bumps

Demonstrated

- Successful probing with single-channel Wide-I/O probe card on Cascade Microtech CM300 probe station
- Limited probe marks on micro-bumps: Cu and Cu/Ni/Sn (after reflow)
- No measureable impact of probing on stacking yield
- 3D-COSTAR: Economic feasibility in single-site testing
NanoPierce™ TSV Contact Solution (FormFactor)

- Socket contacts
- Down to 20 µm array pitch
- Flexible film with many nanofibers
**TSV Probing for Die Logic Testing (Duke Univ.)**

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<tr>
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<tbody>
<tr>
<td>Chakrabarty et al.</td>
<td>Date of Patent: Jul. 15, 2014</td>
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<tr>
<th>(54) SCAN TEST OF DIE LOGIC IN 3D ICS USING TSV PROBING</th>
</tr>
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<tbody>
<tr>
<td>Applicant: <strong>Duke University</strong>, Durham, NC (US)</td>
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<tr>
<td>Inventors: <strong>Krishnendu Chakrabarty</strong>, Chapel Hill, NC (US); <strong>Brandon Noia</strong>, Durham, NC (US)</td>
</tr>
<tr>
<td>Assignee: <strong>Duke University</strong>, Durham, NC (US)</td>
</tr>
<tr>
<td>Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 128 days.</td>
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</table>

**OTHER PUBLICATIONS**


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Noia et al., *IEEE Trans. VLSI Systems*, 2015
Non-Invasive Pre-Bond TSV Test

*(Deutsch and Chakrabarty, TCAD 2014, ITC 2015)*

\[ C = 60 \text{ fF} \]
\[ R_O = 0 \ldots 3 \text{ k}\Omega \]
\[ R_L = 0 \ldots 10 \text{ k}\Omega \]

a) Fault-free case: lumped capacitor \( C = 60 \text{ fF} \)
   \( (R_{TSV} < 1 \text{ \Omega} \rightarrow \text{neglect } R_{TSV}) \)

b) Resistive open fault: \( R_O = 0 \ldots 3 \text{ k}\Omega \text{ at the location } x \)

c) Leakage fault: \( R_L = 0 \ldots 10 \text{ k}\Omega \)

**Main idea:** parametric test for \( R_O \) and \( R_L \)
Ring Oscillator Configuration

Functional circuitry:

Design-for-Test extension:
Ring Oscillator Configuration

- Measure difference $\Delta T = T_1 - T_2$ to reduce inaccuracy due to random process variations
- $\Delta T$ sensitive to defects in TSVs
  - $\Delta T \downarrow$ if resistive open
  - $\Delta T \uparrow$ if leakage
Using Duty Cycle for Pre-Bond TSV Test

**Definitions:**
- Oscillation period: $T_{osc} = T_{on} + T_{off}$
- Duty cycle: $D = \frac{T_{on}}{T_{on} + T_{off}}$

---

**Fault-free**
($G_L = 0, R_O = 0$)
\[
D \approx 0.5
\]

**Leakage fault**
($G_L > 0$)

**Resistive-open fault**
($R_O > 0$)

---

$T_{on}$ increases, $T_{osc}$ increases, $D$ decreases

$T_{off}$ increases, $D$ unchanged

---

$T_{on}$ decreases, $T_{osc}$ unchanged

$T_{off}$ decreases, $D$ decreases
Regression Model Based on Artificial Neural Networks

- **Objective**: determine fault type and size based on measurements
- Use artificial neural networks (ANNs):
  - Efficient for complex systems with large number of inputs
  - Require sufficient number of samples for training

Generic ANN architecture:

Input layer --- Hidden layer --- Output layer

Neurons:

\[ F(\Sigma w_i \alpha_i) \]

Common transfer functions:

- Pure linear \( F(\xi) = \xi \)
- Sigmoid \( F(\xi) = \frac{1}{1+\exp(-\xi)} \)
Regression Model Based on ANN

- **Class-net**: classification network to determine fault type
- **$G_L$-net**: function-fitting network to determine $G_L$
- **$R_O$-net**: function-fitting network to determine $R_O$

- **Inputs**: $\{T_{osc}, T_{osc,b}, D, D_b\}$ measured at $K$ voltage levels
- Two sets of training and test data (10,000 MC samples each)

- $K = 8$ ($V_{dd} = 0.85 \ldots 1.2V$)

- $G_L$ from 0 (fault-free) to 450 $\mu$S (strong leakage)

- $R_O$ from 0 (fault-free) to 5000 $\Omega$ (strong resistive open)
Evaluation of Class-net

1. Train Class-net using training sample set

2. Predict fault class using Class-net for evaluation sample set

3. Compare output class with actual (target) class for each sample
# Evaluation of Class-net

Confusion matrix:

<table>
<thead>
<tr>
<th>Output Class</th>
<th>Target Class</th>
<th>class_leak</th>
<th>class_open</th>
<th>class_dual</th>
</tr>
</thead>
<tbody>
<tr>
<td>class_leak</td>
<td>9524 (33.3%)</td>
<td>58 (0.2%)</td>
<td>0 (0.0%)</td>
<td></td>
</tr>
<tr>
<td>class_open</td>
<td>37 (0.1%)</td>
<td>9818 (34.4%)</td>
<td>135 (0.5%)</td>
<td></td>
</tr>
<tr>
<td>class_dual</td>
<td>0 (0.0%)</td>
<td>124 (0.4%)</td>
<td>8865 (31.0%)</td>
<td></td>
</tr>
</tbody>
</table>

- **Correct prediction**
- **Misprediction**

→Number of mispredictions is relatively small
Evaluation of $G_L$-net and $R_O$-net

$T_{osc}$ alone good enough as input parameter?

- Comparison with models using only oscillation period
- All models trained using same training data set

\[
K \times \{T_{osc}, T_{osc,b}, D, D_b\} \rightarrow G_L\text{-net} \rightarrow G_L
\]
\[
K \times \{T_{osc}, T_{osc,b}\} \rightarrow G_L\text{-net}_r \rightarrow G_L
\]
\[
K \times \{T_{osc}, T_{osc,b}, D, D_b\} \rightarrow R_O\text{-net} \rightarrow R_O
\]
\[
K \times \{T_{osc}, T_{osc,b}\} \rightarrow R_O\text{-net}_r \rightarrow R_O
\]

- Performance evaluation metric: mean squared error (MSE)

\[
MSE = \frac{1}{N} \sum_{i=1}^{N} (y_{p,i} - y_{t,i})^2
\]

- $y_{p,i}$ target value
- $y_{t,i}$ predicted value
Evaluation of $G_L$-net

Error histograms of $G_L$-net and $G_L$-net_r at $G_L = 100$ $\mu$S.

$\rightarrow$ $G_L$-net more accurate (less spread around zero error)
Evaluation of $G_L$-net

- MSE of $G_L$-net and $G_L$-net_r for different values of $G_L$.

\[ MSE = \frac{1}{N} \sum_{i=1}^{N} (y_{p,i} - y_{t,i})^2 \]

→ using $D$ as additional input increases diagnosis accuracy for weak leakage (<100 µS)
Do we need to test at multiple voltage levels?

→ improved diagnosis accuracy using multiple voltage levels
Conclusions

- 3D fabrication and assembly steps (TSVs, alignment, bonding, thinning, etc.) lead to unique defects
- Known test methods can be utilized (extended) for some problems
  - Post-bond test access, IEEE P1838
- Out-of-the-box thinking needed for other test challenges
  - Pre-bond testing (KGD, TSV testing, die logic testing)
  - Cost modeling (when and what to test)
Traffic Lights

KGD, Pre-bond test, Probing

Post-bond test access, DfT, optimization, standards

2.5D: interposer, microbumps, RDL

Test flows

Defect understanding, test content

Thermal-aware testing?

Power integrity?

Clock-domain crossings?

BIST?

Repair?

Test compression?

Debug?
Target TSVs in Production Test and Volume Diagnostics?
TSV Redundancy?
Yield Learning for a 3D Stack?